MANIPAL
ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

Manipal School of Information Sciences

Manipal Academy of Higher Education, Manipal

Outcome Based Education (OBE) Framework

Two Year full time Postgraduate Program

Master of Engineering - ME (VLSI Design)

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NATURE AND EXTENT OF THE PROGRAM

An engineering graduate skillset requirement is changing with invent of the new technologies. In particular the impact of VLSI design provides a high employability in the industry. VLSI devices are found everywhere around us. We find advanced VLSI chips in our cars, cell phones, household appliances, cameras, medical devices and many other places.

Master of Engineering - ME (VLSI Design) Program is a comprehensive two-year postgraduate program, which aims to provide hands-on experience to prepare industry-ready VLSI design professionals. The program VLSI design helps engineering graduates to specialize in the field of hardware description languages, simulation techniques, hardware verification methods, foundations of low power design, and Universal Verification Methodology (UVM). Students also get to use Python, perl and shell scripting technologies to learn the best practices of design workflow automation. Elective courses let students choose between System on Chip (SoC) design, analog CMOS IC design and Digital Signal Processing. Depending on one's interests, a student may learn either advanced logic synthesis or physical design (back-end).

Master of Engineering - ME (VLSI Design) postgraduate degree would welcome graduates from electrical stream with 50% mark in qualifying exam. Students after successfully completing the program will get career opportunities as a Design Engineer, Verification Engineer, CAD Engineer, Application Engineer.

PROGRAM EDUCATION OBJECTIVES (PEO)

The overall objectives of the Learning Outcomes-based Curriculum Framework (LOCF) for **Master of Engineering - ME (VLSI Design) program are as follows.**

PEO No	Education Objective
PEO 1	Successfully engage in challenging careers with professional approach in the areas of analog & digital VLSI design and related domains of engineering.
PEO 2	Demonstrate competence in identifying and analyzing technical problems, suggest feasible and innovative solutions using their core competence in VLSI design and thereby support the technological growth of the nation.
PEO 3	Impart quality technical education, engage in research and contribute to knowledge creation and sharing.
PEO 4	Possess analytical, communicative and leadership skills, and demonstrate the ability to work in multidisciplinary and multi-cultural environments.
PEO 5	Be Self-motivated and remain continuously employable by engaging in lifelong learning.

GRADUATE ATTRIBUTES

S No.	Attribute	Description
1	**Scholarship of Knowledge**	Acquire in-depth knowledge of specific discipline or professional area, including wider and global perspective, with an ability to discriminate, evaluate, analyse and synthesise existing and new knowledge, and integration of the same for enhancement of knowledge.
2	**Critical Thinking**	Analyse complex engineering problems critically, apply independent judgement for synthesising information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.
3	**Problem Solving**	Think laterally and originally, conceptualise and solve engineering problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.
4	**Research Skill**	Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyse and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.
5	**Usage of modern tools**	Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.
6	**Collaborative and Multidisciplinary work**	Possess knowledge and understanding of group dynamics, recognise opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve

		common goals and further the learning of themselves as well as others.
7	**Project Management and Finance**	Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors.
8	**Communication**	Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.
9	**Life-long Learning**	Recognise the need for, and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.
10	**Ethical Practices and Social Responsibility**	Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.
11	**Independent and Reflective Learning**	Observe and examine critically the outcomes of one's actions and make corrective measures subsequently, and learn from mistakes without depending on external feedback.

QUALIFICATIONS DESCRIPTORS

1. Demonstrate

   (i) A systematic, extensive, coherent knowledge and understanding of an academic field of study as a whole and its applications, links to related disciplinary areas/subjects of study; including a critical understanding of the established theories, principles, concepts, and of a number of advanced, emerging issues in the field of VLSI;

   (ii) Procedural knowledge that creates different types of professionals related to the design, fabrication, testing, verification, including research and development, teaching, government and public service.

   (iii) Professional and communication skills in the domain of electronics, IC fabrication, testing, verification, including a critical understanding of the latest developments, and an ability to use established techniques in the domain of VLSI.

2. Demonstrate comprehensive knowledge about materials, including current research, scholarly, and/or professional literature, relating to essential and advanced learning areas pertaining to the VLSI field of study, techniques and skills required for identifying problems and related issues.

3. Demonstrate skills in identifying information needs, collection of relevant quantitative and/or qualitative data drawing on a wide range of sources, analysis and interpretation of data.

4. Methodologies as appropriate to the subject(s) for formulating evidence based solutions and arguments

5. Use knowledge, understanding and skills for critical assessment of a wide range of ideas and complex problems and issues relating to the chosen field of study.

6. Communicate the results of studies undertaken in an academic field accurately in a range of different contexts using the main concepts, constructs and techniques of the VLSI studies.

7. Address one's own learning needs relating to current and emerging areas of study, making use of research, development and professional materials as appropriate, including those related to new frontiers of knowledge.

8. Apply one's disciplinary knowledge and transferable skills to new/unfamiliar contexts and to identify and analyse problems and issues and seek solutions to real-life problems.

PROGRAM OUTCOMES

After successful completion of Master of Engineering - ME (VLSI Design), Students will be able to:

PO No	Attribute	Competency
PO 1	**Scholarship of Knowledge**	Acquire in-depth knowledge of VLSI domain, with an ability to discriminate, evaluate, analyze, synthesize the existing and new knowledge, and integration of the same for enhancement of knowledge.
PO 2	**Critical Thinking**	Analyze complex VLSI Eco System critically, apply independent judgement for synthesizing information to make intellectual and/or creative advances for conducting research in a wider theoretical, practical and policy context.
PO 3	**Problem Solving**	Think laterally and originally, conceptualize and solve VLSI Design problems, evaluate a wide range of potential solutions for those problems and arrive at feasible, optimal solutions after considering public health and safety, cultural, societal and environmental factors in the core areas of expertise.
PO 4	**Research Skill**	Extract information pertinent to unfamiliar problems through literature survey and experiments, apply appropriate research methodologies, techniques and tools, design, conduct experiments, analyze and interpret data, demonstrate higher order skill and view things in a broader perspective, contribute individually/in group(s) to the development of scientific/technological knowledge in one or more domains of engineering.
PO 5	**Usage of modern tools**	Create, select, learn and apply appropriate techniques, resources, and modern engineering and IT tools, including prediction and modelling, to complex engineering activities with an understanding of the limitations.

PO 6	**Collaborative and Multidisciplinary work**	Possess knowledge and understanding of group dynamics, recognize opportunities and contribute positively to collaborative-multidisciplinary scientific research, demonstrate a capacity for self-management and teamwork, decision-making based on open-mindedness, objectivity and rational analysis in order to achieve common goals and further the learning of themselves as well as others.
PO 7	**Project Management and Finance**	Demonstrate knowledge and understanding of engineering and management principles and apply the same to one's own work, as a member and leader in a team, manage projects efficiently in respective disciplines and multidisciplinary environments after consideration of economical and financial factors
PO 8	**Communication**	Communicate with the engineering community, and with society at large, regarding complex engineering activities confidently and effectively, such as, being able to comprehend and write effective reports and design documentation by adhering to appropriate standards, make effective presentations, and give and receive clear instructions.
PO 9	**Life-long Learning**	Recognize the need for and have the preparation and ability to engage in life-long learning independently, with a high level of enthusiasm and commitment to improve knowledge and competence continuously.
PO 10	**Ethical Practices and Social Responsibility**	Acquire professional and intellectual integrity, professional code of conduct, ethics of research and scholarship, consideration of the impact of research outcomes on professional practices and an understanding of responsibility to contribute to the community for sustainable development of society.

PO 11	**Independent and Reflective Learning**	Observe and examine critically the outcomes of one's actions and make corrective measures subsequently and learn from mistakes without depending on external feedback.

COURSE STRUCTURE, COURSEWISE LEARNING OBJECTIVE, AND COURSE OUTCOMES (COS)

FIRST YEAR:

Semester: 1 **Semester: 2**

Subject Code	Subject Title	L	T	P	C	Subject Code	Subject Title	L	T	P	C
CSE 606	Data Structures	3	-	-	3	EDA 604	Advanced VLSI Design	3	-	-	3
EDA 601	High Level Digital Design	3	-	-	3	EDA 605	Low Power VLSI Design	3	-	-	3
EDA 602	Digital Systems & VLSI Design	3	-	-	3	EDA 606	Universal Verification Methodology	3	-	-	3
EDA 603	Verification	3	-	-	3	EDA 607	Scripting for VLSI	3	-	-	3
	Elective - 1	3	-	-	3		Elective - 2	3	-	-	3
CSE 606L	Data Structures Lab	-	-	3	1	EDA 604L	Advanced VLSI Design Lab	-	-	3	1
EDA 601L	High Level Digital Design Lab	-	-	3	1	EDA 605L	Low Power VLSI Design Lab	-	-	3	1
EDA 602L	Digital Systems & VLSI Design Lab	-	-	3	1	EDA 606L	Universal Verification Methodology Lab	-	-	3	1
EDA 603L	Verification Lab	-	-	3	1	EDA 607L	Scripting for VLSI Lab	-	-	3	1
	Elective - 1 Lab	-	-	3	1		Elective - 2 Lab	-	-	3	1
EDA 695	Mini Project - 1	-	-	4	-	EDA 696	Mini Project -2	-	-	-	4
EDA 697	Seminar - 1	-	-	1	-	EDA 698	Seminar - 2	-	-	-	1
Total		**15**	**-**	**15**	**25**	**Total**		**15**	**-**	**15**	**25**

SECOND YEAR (FINAL YEAR):

III and IV Semester		
IOT 799	Project Work	25
Total Number of Credits to Award Degree		75

List of Electives(Theory)

Elective - 1		Elective - 2	
Code	**Subject**	**Code**	**Subject**
EDA-608	System on Chip Design	CSE-615	System Software
EDA-609	CAD for VLSI	CSE-631	IT Project Management
ESD-603	Digital Signal Processing	EDA-610	Physical Design
		EDA-611	Advanced Logic Synthesis
		EDA-612	Formal Methods
		EDA-613	Wireless Communications and Antenna Design
		EDA-614	Machine Learning for VLSI Design
		ENP-601	Entrepreneurship

List of Electives(Lab)

Elective - 1		Elective - 2	
Code	**Subject**	**Code**	**Subject**
EDA-608L	System on Chip Design Lab	CSE-615L	System Software Lab
EDA-609L	CAD for VLSI Lab	CSE-631L	IT Project Management Lab
ESD-603L	Digital Signal Processing Lab	EDA-610L	Physical Design Lab
		EDA-611L	Advanced Logic Synthesis Lab
		EDA-612L	Formal Methods Lab
		EDA-613L	Wireless Communications and Antenna Design Lab
		EDA-614L	Machine Learning for VLSI Design Lab
		ENP-601L	Entrepreneurship Lab

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	**Data Structures**
Course Code: CSE 606	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:** C Programming

Synopsis:	1. This course introduces students to elementary data structures and design of algorithms. 2. Students learn how to design optimal algorithms with respect to time and space 3. Students learn how to implement link list, stack, queues, searching and sorting techniques, sets, trees and graphs. 4. Students learn how to organise the code and write test cases.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Analyse various algorithms
CO 2:	Illustrate programs for implementation of linear data structure like linked list, stack, queue and double linked list
CO 3:	Experiment programs for sorting and searching
CO 4:	Design programs for implementation of non-linear data structure like trees and graph.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*			*							
CO 2	*	*				*					
CO 3	*					*					
CO 4	*	*				*					

Course content and outcomes:

Content	***Competencies***

Unit 1: Introduction	
Algorithm Specification, Performance Analysis .	1. Define algorithms (C1) 2. Analyse algorithms. (C4)
Unit 2: Algorithm Analysis Techniques	
Analysis of Recursive Programs, Solving Recurrence Equations, General Solution for a large class of Recurrences .	1. Define recursive programs (C2) 2. Design simple recursive programs (C6) Solve recurrence relations (C6)
Unit 3: Elementary data structures	
Implementation of Lists, Stacks, Queues	1. Design singly linked list (C6) 2. Design doubly linked list(C6) 3. Explain the concepts of array-based stacks (C2) 4. Explain the concepts of pointer-based stacks (C2) Design and implement Queues. (C6)
Unit 4: Sorting & Searching Techniques	
Quick sort, Heap sort, Merge sort, Binary search, linear search, Fibonacci search	1. Develop algorithm for insertion sort, bubble sort and selection sort. (C6) 2. Develop and analyse algorithm for quick sort (C6) 3. Develop and analyse algorithm for heap sort (C6) 4. Develop and analyse algorithm for merge sort (C6) 5. Design and analyse algorithms for binary, linear and Fibonacci search (C6)
Unit 5: Operations on Sets	
Introduction to Sets, A Linked- List implementation of Set, The Dictionary, The Hash Table Data Structure	1. Develop data structures for sets (C6) 2. Design a linked list-based implementation of sets (C6)

	3. Design a Dictionary (C6) 4. Design Data structure for hash table (C6)
Unit 6: Trees	
Basic Terminology, Implementation of Trees, Binary Trees, Binary Search Trees	1. Examine the concepts of trees. (C3) 2. Design and implement general trees (C6) 3. Design and implement binary trees (C6) 4. Design and implement binary search trees (C6)
Unit 7: Graphs	
Basic definitions, Representation of Graphs, Minimum Cost Spanning Tree, Single Source Shortest Paths, All-Pairs Shortest Path	1. Define graphs (C6) 2. Design data structure for graphs (C6) 3. Formulate an algorithm to solve minimum cost spanning tree(C6) 4. Formulate an algorithm to solve Single source shortest path (C6) 5. Formulate an algorithm to solve All- pair shortest path(C6)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*	*		
Sessional Examination 2		*	*	*
Assignment/Presentation	*	*	*	*
End Semester Examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Introduction to Algorithms" Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. 2. "Data Structures& Algorithms" Aho, Hopcroft and Ulmann 3. "Data structures and algorithm analysis in C" Mark Allen Weiss

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	High Level Digital Design
Course Code: EDA-601	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:**

Synopsis:

This Course provides insight on

1. To understand number representation and conversion between different representation in digital electronic circuits.
2. To analyze logic processes and implement logical operations using combinational logic circuits.
3. To understand characteristics of memory and their classification.
4. To understand concepts of sequential circuits and to analyze sequential systems in terms of state machines.
5. To understand concept of Programmable Devices, PLA, PAL, CPLD and FPGA and implement digital system using SystemVerilog.
6. To understand the AMBA bus protocol and types of buses

Course Outcomes (COs):

On successful completion of this course, students will be able to

CO 1:	Develop a digital logic and apply it to solve real life problems.
CO 2:	Analyse, design and implement combinational, sequential logic circuits.
CO 3:	Discuss different semiconductor memories.
CO 4:	Analyse digital system design using PLD.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1		*									
CO 2			*								
CO 3	*										
CO 4	*										

Course content and outcomes:

Content	*Competencies*
Unit 1: Introduction	
Review of Digital Design	1. Discuss number system in digital design. (C2) 2. Discuss Boolean algebra in digital design. (C2) 3. Optimize the Boolean expression using k-maps. (C3)
Unit 2: Combinational circuits - Design steps	
Arithmetic Circuits - Full adder, Serial Adder, Adder/Subtractor, Ripple Carry Chain, Carry Look-Ahead adder, Carry Select Adder, ALU, Parity Generator, Comparator, Multiplier. PLA, PAL, PLD, CPLD, ROM, FPGA – Introduction	1. Design a combinational circuit for a given boolean expression (C5). 2. Discuss different types of combinational circuits like adders, multipliers and CPLD's. (C2)
Unit 3: Sequential circuits - Design steps	
Flip-flops, registers, counters.	1. Design sequential circuit using Flip-flops (C5)
Unit 4: Finite State Machines	
Introduction to FSMs, capabilities, minimization and transformation of sequential machines, Synchronous and asynchronous FSMs, Mealy and Moore machines, State assignment of synchronous sequential machines, Structure of sequential machines, Verification and testing of sequential circuits	1. Discuss Mealy and Moore machines (C2) 2. Design sequential circuit using Mealy and Moore machines (C5)
Unit 5: Verilog / System Verilog for design	
Verilog / System Verilog for design	1. Differentiate Verilog and System Verilog. (C4)
Unit 6: Introduction FPGA	
Introduction FPGA	2. Explain FPGA architecture. (C2)

Unit 7: Spartan III Architecture	
Spartan III Architecture	3. Discuss Spartan III Architecture. (C2)
Unit 8: Application on Digital Design	
FIFO Design [SNUG Paper], Cordic Algorithm [IEEE Paper] Floating Point Arithmetic Blocks [IEEE Paper]: Floating point Addition, Floating point, subtraction, Floating point Multiplication, Floating point Division	1. Explain the working of FIFO (C2) 2. Explain cordic algorithm (C2) 3. Discuss different floating-point arithmetic operations (C2)
Unit 8: AMBA Bus Specification [ARM Specification]	
AMBA Bus Specification [ARM Specification]	1. Discuss different components of AMBA bus (C2) 2. Explain AHB and APB (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination

Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*	*		
Sessional Examination 2			*	*
Assignment/Presentation				*
End Semester Examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• "An Engineering Approach to Digital Design" , Flectcher • "SystemVerilog for design by Stuart Sutherland" , Simon Davidmann, Peter Flake • SNUG Paper [freely available] • IEEE Paper [MU campus available] • ARM Specification.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Digital Systems & VLSI Design
Course Code: EDA 602	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:**

Synopsis:	This Course provides insight on
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Understand static and dynamic behaviour of MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) and the secondary effects of the MOS transistor model.
CO 2:	Design and test static CMOS combinational and sequential logic at the transistor level, including mask layout.
CO 3:	To provide experience designing integrated circuits using Computer Aided Design (CAD) Tools
CO 4:	Describe the general processing technologies of CMOS integrated circuits.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1		*									
CO 2	*	*	*								
CO 3				*							
CO 4			*								

Course content and outcomes:

Content	***Competencies***
Unit 1: MOS transistor theory	

Ideal I-V Characteristics, C-V Characteristics, CMOS inverter – DC characteristics, , Noise Margin, Static load MOS inverters, NELS, NELT, HMOS, Pass transistor, Transmission gate, tristate inverter, MOSFET Models, Non ideal I-V effects.	1. Illustrate basic working of MOS transistors (C4) 2. Design construction of basic building block (C5)
Unit 2: CMOS circuit and layout design	
Combinational and Sequential Circuit Design, Basic physical design of simple gates, CMOS logic structures (Dynamic CMOS Logic, C2MOS Logic, CMOS and NP Domino Logic).	1. Illustrate development basic logic gates using MOSFET (C4) 2. Design Construction of static and dynamic logic circuits (C5)
Unit 3: Circuit characterization	
Resistance estimation, Capacitance estimation, delay time calculation, principles of modeling the gate, Switching characteristics, CMOS gate transistor sizing, Power dissipation, Scaling principles.	1. Analysis of MOS circuits – RLC estimation (C4) 2. Estimation of power dissipation in MOS circuits (C6)
Unit 4: CMOS Subsystem Design	
Data path operations - Adder, Comparator, Counter, Semiconductor memory elements - SRAM, DRAM	1. Design simple CMOS subsystem (C5)
Unit 5: CMOS Technologies	
Wafer Formation, Photolithography, Well and Channel Formation, Silicon Dioxide (SiO2), Oxidation, Isolation Gate Oxide, Gate and Source/Drain	1. Demonstrate basic CMOS process technologies (C3) 2. Demonstrate design rules and layout techniques for simple digital CMOS circuits (C3)

Formations, Contacts and Metallization, Passivation, SOI.	
Unit 6: Layout Design Rules	
Design Rule Background, Micron and Lambda Design Rules	1. Demonstrate layout design rules (C3)
Unit 7: Manufacturing Issues	
Antenna Rules, Layer Density Rules, Resolution Enhancement Rules.	1. Demonstrate various manufacturing issues (C3)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*	*		

Sessional Examination 2			*	*
Assignment/Presentation				*
End Semester Examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. ”CMOS digital integrated circuits analysis and design”, Kang Sung Mo and Leblebici Yusuf, McGraw Hill, 1999. 2. “Principles of CMOS VLSI Design: A systems perspective”, 2nd Edition, Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1999. 3. “CMOS VLSI Design: A circuits & systems perspective”, 3rd Edition, Neil H. E. Weste, David Harris, Addison Wesley, 2007. 4. “Microchip Fabrication”, by Peter Van Zant, 5th Edition, McGraw-Hill, International Edition.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Verification
Course Code: EDA 603	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:**

Synopsis:	This Course provides insight on 1. To study the basic concepts of system verilog. 2. To understand different kinds of data types. 3. To Differentiate between HDL and HVL. 4. To Study the basic concepts of OOPs. 5. To understand the different components of verification environment.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Design a scenario for Verification of a DUT in System Verilog.
CO 2:	Analyze the usefulness of a driver, monitor, checker, test cases in a verification environment.
CO 3:	Explain the concept of randomization and its importance in verification coverage in a bigger design.
CO 4:	Design test bench to verify the functionality of a design.
CO 5:	Design a VIP for an IP as a project.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*								
CO 2		*									
CO 3	*										
CO 4			*	*							
CO 5			*	*							

Course content and outcomes:

Content	*Competencies*
Unit 1: Introduction	
Verification Productivity, Verification, Design for Verification, Methodology.	1. What is verification? Differentiate basic V design and modified V design (C4)
Unit 2: Types of Verifications & Approaches	
Formal Verification, Property Based Verification, Functional Verification, Rule Checking-Linting, Black Box Verification, White Box Verification, Grey Box Verification.	1. Explain different types of verification (C2)
Unit 3: Verification Planning	
Planning Process, Response Checking	1. Explain verification planning process (C2)
Unit 4: Assertions	
Specifying Assertions, Assertions on Internal DUT Signals, Assertions on External Interfaces, Assertion Coding Guidelines, Reusable Assertion-Based, Qualification of Assertions.	1. What is assertion? Explain different types of assertions in System Verilog. (C2)
Unit 5: Testbench Infrastructure:	
Testbench Architecture, Simulation Control, Data and Transactions, Transactors, Transaction-Level Interfaces, Timing Interface, Callback Methods, Ad-Hoc Testbenches, Legacy Bus-Functional Model.	1. Explain components of verification environment. (C2) 2. Explain data and transactions. (C2) 3. Explain transaction-level interfaces and timing interfaces. (C2) 4. Explain Ad-hoc testbenches and Bus Functional Models. (C2)

Unit 6: Stimulus and Response	
Generating Stimulus, Controlling Random Generation, Self-Checking Structures.	1. Explain self-checking structures in verification (C2)
Unit 7: Coverage-Driven Verification	
Coverage Metrics, Coverage Models, Functional Coverage Implementation, Feedback Mechanisms	1. Explain coverage metrics and coverage models in System Verilog. (C2)
Unit 8: Assertions for Formal Tools	
Model Checking and Assertions, Assertions on Data	1. Explain how assertions can be used during formal verification (C2)
Unit 9: System-Level Verification	
Extensible Verification Components, XVC Manager, System-Level Verification Environments, Verifying Transaction-Level Models, Hardware-Assisted Verification.	1. Explain system-level verification environment. (C2)
Unit 10: Processor Integration Verification	
Software Test Environments, Structure of Software Tests, Test Actions.	1. Explain software test environment and test actions (C2)
Unit 10: Post-Silicon SoC Validation	
Introduction, Validation Activities, Planning for Post-Silicon Readiness, Post-Silicon Debug Infrastructure, Generation of Tests, Post-Silicon Debug.	1. Computing post-silicon validation (C3) 2. Explain the debug infrastructure for post-silicon validation (C2)
Learning strategies, contact hours and student learning time	

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Sessional Examination 1	*	*			
Sessional Examination 2			*	*	
Assignment/Presentation					*
End Semester Examination	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Janick Bergeron, Verification methodology manual for SystemVerilog, Springer. 2. Janick Bergeron, Writing Testbenches using System Verilog, Springer.

	3. William K. Lam, Hardware Design Verification - Simulation and Formal Method Based Approaches. 4. Pallab Dasgupta, A Roadmap for Formal Property Verification, Springer. 5. Prabhat Mishra, Farimah Farahmandi, Post-Silicon Validation and Debug, Springer.

MANIPAL
ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	System-on-Chip Design
Course Code: EDA-608	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:** Basic knowledge of Computer Architecture, C programming language

Synopsis:	This Course provides insight on 1. The concept of systems approach towards electronic system level flow 2. System on chip architecture with data processing, data storage, communications and control mechanisms 3. The concept of various processor architectures 4. Various memory architectures 5. Concept of buses, layered architecture and network on chip 6. 3-D graphics processors and universal serial bus
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe system architecture, identify hardware software co-design, give examples of co-design space, explain specification & modelling, pre-partition, partition, analyse post-partition analysis, describe hardware and software implementation
CO 2:	Review the processors and its micro-architecture and basic elements in instruction handling, recognize robust processors
CO 3:	Describe on and off-die memories, explain memories in system on chip, compare memory systems, cache memory, model memories, interconnects in system on chip, explain network on chip

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										

CO 2		*									
CO 3	*		*								

Course content and outcomes:

Content	***Competencies***
Unit 1: Introduction to System Approach:	
Introduction to System Approach: System Architecture overview, Components of the System, Introducing Hardware/Software Codesign, The Driving Factors of Hardware/Software Design, The Hardware-Software Codesign space.	1. Explain system on chip (C2) 2. Describe hardware software co-design (C2) 3. Explain driving factors of co-design (C2)
Unit 2: Electronic System Level Flow	
Specification and Modeling, Pre-Partitioning Analysis, Partitioning, Post-Partitioning Analysis and Debug, Post-Partitioning Verification, Hardware Implementation, Software Implementation.	1. Explain specification and modelling (C2) 2. Describe pre-portioning analysis (C2) 3. Defend partition steps (C2) 4. Analyse post-partition and verification(C4) 5. Explain hardware and software implementation (C2)
Unit 3: Design Principles in SOC Architecture	
Heterogeneous & Distributed Data Processing, Heterogeneous & Distributed Data Communications, Heterogeneous & Distributed Data Storage, Hierarchical Control.	1. Describe Heterogeneous & Distributed Data Processing (C2) 2. Describe Heterogeneous & Distributed Data Communications (C2) 3. Explain Heterogeneous & Distributed Data Storage (C2) 4. Discuss Hierarchical Control (C2)

Unit 4: Processors	
Processors: Introduction to Processors, Processor Selection for SOC, Basic Concepts in Processor Architecture, RISC Pipeline, Basic Concepts in Processor Microarchitecture, Basic Elements in Instruction Handling, Buffers, Branches, Robust Processors	1. Explain processors in system on chip (C2) 2. Identify processor Selection for system on chip (C4) 3. Describe basic concepts in processor architecture (C5) 4. Describe RISC pipeline architecture (C1) 5. Recognize basic elements in instruction handling (C1) 6. Explain buffers, branches and robust processors (C2)
Unit 5: Memory Design	
Introduction, Overview of SOC Internal and External Memories, Scratchpads and Cache Memory, Cache Organization, Cache Data, Write Policies, Strategies for Line Replacement at Miss Time, Other Types of Caches, Split I- and D-Caches and the Effect of Code Density, Multilevel Caches, Virtual-to-Real Translation, SOC (On-Die) Memory Systems, Board-Based (Off-Die) Memory systems, Simple DRAM and the Memory Array, Models of Simple Processor-Memory Interaction.	1. Describe memories (C2) 2. Compare On and Off die memories (C4) 3. Model memories (C4)
Unit 6: Hardware Interconnects	
Introduction, Overview of Interconnect Architectures, Bus Architecture, SOC	1. Define buses in system on chip (C1) 2. Give examples of system on buses (C2)

Standard Buses, Analytic Bus Models, Beyond the Bus (NOC with Switch Interconnects), Some NOC Switch Examples, Layered Architecture and Network Interface Unit, Evaluating Interconnect Networks.	3. Analyse bus models (C4) 4. Explain network on chip (C2)
Unit 7: Hardware/Software Interfaces	
Introduction, Synchronization Schemes, Memory-Mapped Interfaces, Coprocessor Interfaces, Custom-Instruction Interfaces.	1. Identify synchronization schemes (C4) 2. Explain memory-mapped interfaces (C2) 3. Describe coprocessor interfaces (C2) 4. Explain custom-instruction interfaces (C2)
Unit 8: Application Studies	
3-D Graphics Processor / Software Defined Radio with 802.16, Universal Serial Bus	1. Explain 3-D graphics processor/software defined radio with 802.16, universal serial bus (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:	
Formative:	**Summative:**

Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*		
Sessional Examination 2		*	*
Assignment/Presentation			*
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Michael J. Flynn , Wayne Luk, "Computer System Design System-On-Chip", John Wiley & Sons, Inc., Publication, 2011. 2. Brain Bailey, Grant Martin, Andrew Piziali, "ESL Design and Verification: A Prescription for Electronic System-Level Methodology", Morgan Kaufmann Publication, 2007. 3. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Codesign", Springer, 2010. 4. Don Anderson, USB System Architecture (USB 2.0), Mindshare, Inc., 2001.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	CAD for VLSI
Course Code: EDA-609	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:** Basic understanding of VLSI Design, Digital design, Graph theory, Data structures

Synopsis:	This Course provides insights on 1. VLSI design fllows 2. VLSI design automation at various stages of IC design, verification and testing 3. Various EDA tools used in VLSI design 4. VLSI design problems and developing CAD tools to address these 5. Algorithms used in the CAD tools for VLSI design and optimization
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Understand VLSI design flows
CO 2:	Apply design automation tools used in VLSI design
CO 3:	Infer important design problems in VLSI and developing tools to address them
CO 4:	Understand various algorithms used in EDA tools and using them for VLSI CAD tool development

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2			*								
CO 3		*		*							
CO 4					*						

Course content and outcomes:

Content	***Competencies***
Unit 1: Layout Compaction	

Design rules, symbolic layout, Algorithms for layout compaction.	At the end of the topic student should be able to: 1. Explain the basics of layout and relevant tools (C2)
Unit 2: Placement and Partitioning	
Circuit representation, Wire length estimation, Types of placement problems, Placement algorithms, and partitioning algorithms	1. Model circuits using graphs (C4) 2. Recognize placement and partitioning stages apply algorithms to solve problems in those tasks (C2)
Unit 3: Floor planning	
Floor planning concepts, Shape Functions and Floor plan sizing	1. Describe role of floor planning and optimization (C2)
Unit 4: Routing	
Global routing, algorithms for global routing, local routing, types of local routing problems, Area Routing, algorithms for area routing, Channel routing, algorithms for channel routing.	1. Apply Mapping of routing problems into graph domain (C3) 2. Illustrate channel routing problems and apply algorithms to solve routing problems (C3)
Unit 5: Logic synthesis and verification	
Introduction to Combinational logic synthesis, Binary decision diagrams, ITE & ITE-CONTSNT algorithm in two level logic synthesis	1. Apply ITE algorithm in logic synthesis (C3)
Unit 6: High level logic synthesis	
Need for high-level logic synthesis, Design representation and Transformations, Partitioning, Scheduling, Allocation.	1. Describe of high level synthesis (C2) 2. Illustrrate design reperesentations (C3) 3. Formulate synthesis poblems – Partitioning, scheduling, allocation (C5)

	4. Employ standard algorithms to solve high level syntheis tasks (C3)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*			
Sessional Examination 2		*		
Assignment/Presentation			*	*
End Semester Examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. “Graph theory” , Narsingh Deo (Prentice-Hall of India private ltd)

	2. “Graph theory” , Gibbons 3. “Algorithms for VLSI Design Automation” , Sabih H. Gerez (John Wiley and Sons) 4. “High Level Synthesis -Introduction to chip and System Design” , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers) 5. “Logic synthesis and verification algorithms” , Gary D. Hachtel, Fabio Somenzi (Kluwer Academic Publishers) 6. “Computer aided logical design with emphasis on VLSI “ , Frederick J Hill, Gerald R. Peterson (john Wiley & sons)

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Digital Signal Processing
Course Code: ESD-603	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 1
No of Credits: 3	**Prerequisites:** Knowledge of Signals and Systems and Basic Knowledge of MATLAB

Synopsis:	This Course provides insight on 1. Understanding of basics of Signal and Systems as pre-requisite. 2. Understanding the concepts of Fast Fourier Transforms. 3. Learning hardware implementation of systems. 4. Learning FIR and IIR Filter Designs. 5. Learning concepts of multi-rate signal processing in the form of sampling rate conversion, structures of sampling rate converters and some applications of sampling rate converters 6. Understanding three optimum Weiner filters, adaptive algorithm and transforming Weiner filters in to adaptive filters 7. Understanding architecture, memory management and pipelining concepts of TMS320C67XX processor through self-stud.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Analyse Fast Fourier Transform (FFT) algorithms on computational complexity.
CO 2:	Describe the structures for IIR and FIR filters.
CO 3:	Interpret Multirate Signal Processing and Adaptive Filters.
CO 4:	Explain architecture, memory management and pipelining concepts of General and TMS320C67XX Digital Signal Processor.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*	*		*						

CO 2	*	*	*	*	*						
CO 3		*	*	*							
CO 4	*	*									

Course content and outcomes:

Content	***Competencies***
Unit 1: Review: (Self Study)	
Introduction Classification of signals and systems, brief discussions on z-transform, inverse z-transform & Fourier transform, DFT, linear convolution using circular convolution & DFT	1. Outline types of signals and system. (C1) 2. Summarize z-transform, Fourier transform, convolution. (C2)
Unit 2: FFT Algorithms	
Radix-2 DIT-FFT Algorithm, DIF-FFT Algorithm. Assignments (Problems).	1. Identify Computation complexity of DFT, Introduction to Fast Fourier Transform (FFT) algorithm (C1) 2. Describe and Sketch Radix-2 Decimation in Time FFT (DIT-FFT) Algorithm and analyse its computation complexity (C2, C3, C4) 3. Describe and Sketch Radix-2 Decimation in Frequency FFT (DIF-FFT) Algorithm and analyse its computation complexity (C2, C3, C4)
Unit 3: Filter Structures	
IIR Filter Structure – Direct Form I & II, CSOS, PSOS & Transpose structures - FIR Filter Structures – Direct Form, Cascade form, Linear Phase Filter structures. Assignments (Problems).	1. List Components used in filter structures, System Representations, relation between the representations, classify of IIR and FIR Systems (C1, C2) 2. Explain and construct IIR Filter Structure – Direct Form-I, Direct Form–II, Cascade Form

	(CSOS), Parallel Form (PSOS) & Transpose of structures (C2, C5) 3. Explain and construct FIR Filter Structures – Direct Form, Cascade form (C2, C5) 4. Explain Linear Phase FIR Filter structure: Derivation, Frequency Response, Compute Computation Complexity and construct with number of filter coefficients being even and odd. (C3, C5)
Unit 4: Design of FIR filters	
Using Frequency Sampling & Windows - Assignments (Problems).	1. Introduction to Frequency sampling technique design 2. Describe Derivation of a Transfer Function for the system designed using frequency sampling technique when number of samples of impulse response / number of point DFT is even or odd. Construct hardware for the transfer functions. Concept of Comb filter and resonator (C6, C5) 3. Sample example to Design and implement FIR filter using Frequency Sampling technique to meet required impulse response (C5, P4) 4. Illustrate Frequency responses of frequency selective (LP, HP, BP and BR) filters, concept of frequency sampling in the frequency responses (C3) 5. Sample examples to Design and implement FIR filters with ideal frequency response using frequency sampling technique (C5, P4) 6. Discuss Concept of windowing in the design of FIR filter, Concept of Gibb's Phenomenon and

	its effect on frequency response, Use of window functions to eliminate Gibb's effect (C2) 7. Comparison of performances of filters designed with different window functions (C4) 8. Explain Steps involved in the design of FIR filters with ideal frequency response and non-ideal frequency response (C2) 9. Express Impulse responses of frequency selective filters (C2) 10. Sample examples to design ideal and non-ideal frequency selective filters using windows. (C5, P4)
Unit 5: Design of IIR Filters	
Butterworth & Chebychev filters design using impulse invariance & bilinear transformation techniques, Design of IIR filter using pole placement technique. Assignments (Problems).	1. Discuss Concepts of Analog Butterworth LP filter, concept of Cut-off frequency, order of the filter, compute poles, pole locations in S-Plane, transfer function (C2, C3) 2. Explain Design steps of Analog Butterworth LP filter (C2) 3. Explain Chebychev polynomials, their properties, Analog Chebychev LP filter function, concepts of frequency response, order of filter, pole placements of Chebychev LP filters on S-Plane, compute poles, Transfer function of LP Chebychev filter (C2, C3) 4. Discuss Concepts of Impulse Invariance Transformation, S-Plane to Z-Plane mapping, steps in transformation (C2)

	5. Discuss Concepts of Bilinear Transformation, frequency warping, pre-warping for the purpose of analog filter (Butterworth / Chebychev) design (C2) 6. Sample examples to design Butterworth and Chebychev LP filter using impulse invariance and bilinear transformations (C5)
Unit 6: Multirate Signal Processing	
Decimation, Interpolation, Sampling rate conversion by a rational factor, structures, Polyphase filter structures, Time variant Filter structure, Application of Multirate signal processing to Phase Shifter, Subband coding of Speech signal, Digital Filter Bank Implementation, QMF Filter bank	7. Introduction, need for multi-rate signal processing, explain concept of sampling rate conversion (C2) 8. Explain Decimation by an integer factor, block diagram, analyse of decimator in time domain and frequency domain (C2) 9. Explain Interpolation by an integer factor, block diagram, analyse of interpolator in time domain and frequency domain (C2) 10. Explain Sampling rate conversion by a rational factor, block diagram, analyse in time domain and frequency domain (C2) 11. Construct Implementation of Sampling rate converters (C5) 12. Discuss Concepts and construction of Poly-phase filter (C2) 13. Construct Time variant Filter (C5) 14. Apply Multi-rate signal processing concept to Phase Shifter, Sub-band coding of Speech signal, Digital Filter bank Implementation, QMF Filter bank. (C3)
Unit 7: Adaptive Filters	

Class of Optimal Filters – Predictive Configuration, Filter Configuration, Concept of adaptive noise cancellation, Noise Canceller Configuration. LMS adaptive Algorithm, Application of LMS algorithm to the optimal filter configurations. Adaptive noise canceller as a high-pass filter	1. Outline adaptive filters, some matrix operation.(C1) 2. Explain Optimal Weiner Filters – Predictive Configuration, Filter Configuration, Noise Canceller Configuration (C2) 3. Explain Concept of LMS adaptive Algorithm (C2) 4. Apply LMS algorithm to the optimal filter configurations (C3)
Unit 7: DSP Processor	
Introduction to PDSPs – Multiplier and Multiplier Accumulator (MAC), Modified Bus structures and memory access schemes, Multiple access memory, Multiported Memory, VLIW architecture, Pipelining, Special addressing modes, On-chip Peripherals. TMS320C6711 DSP processor: Architecture, Instruction set and assembly language programming	1. Discuss Introduction to PDSPs – Multiplier and Multiplier Accumulator (MAC), Modified Bus structures and memory access schemes (C2) 2. Explain Concept of Multiple access memory, Multiported Memory, VLIW architecture (C2) 3. Explain Concept of Pipelining, Special addressing modes, On-chip Peripherals. (C2) 4. Explain Concepts on Architecture, memory organization and pipelining of TMS320c67XX (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-

Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*	*		
Sessional Examination 2			*	
Assignment/Presentation		*	*	
End Semester Examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Sanjith K Mitra, "Digital Signal Processing", McGraw Hill Education, 4 Edition, July 2013. 2. Oppenheim and Schafer, "Digital Signal Processing", Pearson, First Edition, 1975. 3. Roman Kuc, "Digital Signal Processing", McGraw-Hill Education, 1988. 4. Proakis and Manolakis, "Digital Signal Processing", Prentice – Hall, Inc., Third Edition, 1996. 5. Rabinder and Gold, "Theory and Application of Digital Signal Processing", Prentice Hall India Learning Private Limited, 1988. 6. Hwei P Hsu, Schaum's Outline of "Signals and Systems", 3rd Edition, 2013. 7. Symon Haykins, "Signals and Systems", Wiley, Second Edition, 2002.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Data Structures Lab
Course Code: CSE 606L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:** C Programming

Synopsis:	1. This course introduces students to elementary data structures and design of algorithms. 2. Students learn how to design optimal algorithms with respect to time and space 3. Students learn how to implement link list, stack, queues, searching and sorting techniques, sets, trees and graphs.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Analyse various algorithms.
CO 2:	Illustrate programs for implementation of linear data structure like linked list, stack, queue and double linked list
CO 3:	Experiment programs for sorting and searching
CO 4:	Design programs for implementation of non-linear data structure like trees and graph.
CO 5:	Design the code for scalability and maintainability

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1		*									
CO 2		*	*		*			*			
CO 3		*	*		*			*			
CO 4		*	*		*			*			
CO5:		*	*		*			*			

Course content and outcomes:

Content	*Competencies*
Unit 1: Elementary data structures	
Implementation of Lists, Stacks, Queues	1. Design and Implement singly linked list (C5) 2. Design and Implement doubly linked list (C5) 3. Design and Implement array-based stack (C5) 4. Design and Implement pointer-based stack(C5) 5. Design and Implement array-based queues.(C5) 6. Design and Implement pointer-based queues. (C5)
Unit 2: Sorting & Searching Techniques	
Quick sort, Heap sort, Merge sort, Binary search, linear search, Fibonacci search	1. Design and implement programs for insertion sort, bubble sort and selection sort. (C5) 2. Design and implement programs for quick sort (C5) 3. Design and implement programs for heap sort(C5) 4. Design and implement programs for merge sort (C5) 5. Design and implement programs for binary, linear and Fibonacci search (C5)
Unit 3: Operations on Sets	
Introduction to Sets, A Linked- List implementation of Set, The Dictionary, The Hash Table Data Structure	(C2, C3, C5, C8) 1. Experiment a program for array-based implementation of sets (C4) 2. Experiment a program for linked list-based implementation of sets (C4)

	3. Experiment a program for implementing a dictionary (C4) 4. Experiment programs for implementing open and closed hash tables. (C4)
Unit 4: Trees	
Basic Terminology, Implementation of Trees, Binary Trees, Binary Search Trees	1. Experiment a program to implement binary trees (C4) 2. Experiment a program to implement binary search trees (C4) 3. Experiment Tree traversal techniques (C4)
Unit 5: Graphs	
Basic definitions, Representation of Graphs, Minimum Cost Spanning Tree, Single Source Shortest Paths, All-Pairs Shortest Path	1. Experiment programs to represent a graph using adjacency matrix and adjacency list techniques (C4) 2. Experiment a program to implement minimum cost spanning tree (C4) 3. Experiment a program to solve Single source shortest path problem (C4) 4. Experiment a program to solve All- pair shortest path problem (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-

Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Practice problems	Internal Lab test
Assignment evaluation	End semester Lab examination
	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Sessional Examination 1	*	*			
Sessional Examination 2		*	*	*	
Assignment/Presentation	*	*	*	*	*
Laboratory examination	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Introduction to Algorithms" Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest. 2. "Data Structures& Algorithms" Aho, Hopcroft and Ulmann 3. "Data structures and algorithm analysis in C" Mark Allen Weiss

Name of the Program:	ME in VLSI
Course Title:	High Level Digital Design Lab
Course Code: EDA-601L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:**

Synopsis:

This Course provides insight on

1. To analyze logic processes and implement logical operations using combinational logic circuits and implement digital system using System Verilog.
2. To understand characteristics of memory and their classification and implement digital system using System Verilog.
3. To understand concepts of sequential circuits and to analyze sequential systems in terms of state machines and implement digital system using System Verilog.
4. To understand concept of Programmable Devices, PLA, PAL, CPLD and FPGA and implement digital system using System Verilog.
5. To understand the AMBA bus protocol and types of buses and implement digital system using System Verilog

Course Outcomes (COs):

On successful completion of this course, students will be able to

CO 1:	Design and implement combinational circuits.
CO 2:	Design and implement sequential logic circuits.
CO 3:	Design and implement AMBA Bus protocol.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*		*						
CO 2	*	*	*		*						
CO 3	*		*		*						

Course content and outcomes:	
Content	***Competencies***
Unit 1: Introduction	
Data flow modelling	1. Experiment boolean expression using dataflow modelling.
Unit 2: Combinational circuits - Design steps	
Combinational circuits	1. Experiment combinational circuits like adders, multipliers and CPLD's using System Verilog.
Unit 3: Sequential circuits - Design steps	
Sequential circuits	1. Experiment sequential circuit using System Verilog(C4)
Unit 4: Finite State Machines	
Mealy and Moore machines	1. Experiment Mealy and Moore machines using System Verilog (C4)
Unit 5: Verilog / System Verilog for design	
System Verilog for design	1. Differentiate Verilog and System Verilog. (C4)
Unit 6: Introduction FPGA	
Vertex-5 FPGA	1. Experiment combinational and sequential circuits on Vertex-5 FPGA. (C4)
Unit 7: Spartan III Architecture	
Spartan III Architecture	1. Experiment combinational and sequential circuits on Spartan III. (C4)
Unit 8: Application on Digital Design	
FIFO using system verilog	1. Experiment FIFO using System Verilog(C4)
Unit 8: AMBA Bus Specification [ARM Specification]	
AHB and APB using system verilog	1. Experiment AHB and APB using System Verilog (C4)

Learning strategies, contact hours and student learning time		
Learning strategy	*Contact hours*	*Student learning time (Hrs)*

Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation			*
Lab Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• "An Engineering Approach to Digital Design" , Flectcher • "SystemVerilog for design by Stuart Sutherland" , Simon Davidmann, Peter Flake

	• SNUG Paper [freely available] • IEEE Paper [MU campus available] • ARM Specification.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Digital Systems and VLSI Design Lab
Course Code:	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic Electronics, Digital Systems

Synopsis:	This Course provides insight on 1. To study the basic working of MOSFETs. 2. To Design basic logic gates using MOSFETs. 3. To design simple combinational and sequential circuits. 4. To draw layouts for basic logic gates and simple circuits. 5. To simulate the designs and verify the functionality.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Design and test static CMOS combinational and sequential logic at the transistor level, including mask layout
CO 2:	Design integrated circuits using Computer Aided Design (CAD) Tools

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*	*		*						
CO 2	*	*	*		*						

Course content and outcomes:

Content	***Competencies***
Unit 1: MOS transistor theory	
To plot I-V Characteristics of MOSFET To plot DC characteristics, transfer characteristics of CMOS inverter and compute parameters like noise margin, power dissipation	1. Prepare I-V Characteristics of MOSFET (C3)

Unit 2: CMOS circuit and layout design	
To design basic physical design of simple circuits	1. Design basic physical design of simple circuits (C5)
Unit 3: Circuit characterization	
Verify the Switching characteristics and Power dissipation of CMOS circuits	1. Examine Switching characteristics and Power dissipation of CMOS circuits (C4)
Unit 4: CMOS Subsystem Design	
Design and simulation of simple combinational circuits such as Adders, Comparator, Counter etc.	1. Design simple combinational circuits such as Adders, Comparator, Counter etc. (C5)
Unit 5: Layout Design Rules	
Familiarizing use of EDA tools like Cadence suite to draw and check design rule	1. Experiment with EDA tools like Cadence suite to draw and check design rule (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-

Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2
Sessional Examination 1	*	*
Sessional Examination 2		*
Assignment/Presentation	*	*
Laboratory examination	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Cadence user manual

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Verification Lab
Course Code: EDA 603L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:**

Synopsis:	This Course provides insight on 1. To study the basic concepts of system verilog. 2. To understand different kinds of data types. 3. To Study the basic concepts of OOPs. 4. To understand the different components of verification environment.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Design a scenario for Verification of a DUT in System Verilog
CO 2:	Implement the usefulness of a driver, monitor, checker, test cases in a verification environment
CO 3:	Design test bench to verify the functionality of a design
CO 4:	Design a VIP for an IP as a project

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*								
CO 2	*	*			*						
CO 3			*								
CO 4	*		*								

Course content and outcomes:

Content	***Competencies***
Unit 1: Introduction	
Fundamental functionalities in system verilog	1. Implement interfaces, queue, arrays, task and functions in System Verilog.

Unit 2: Types of Verifications & Approaches	
Oops concepts in system verilog	1. Experiment inheritance, polymorphism, data encapsulation and abstraction in System Verilog (C4)
Unit 3: Verification Planning	
Verification plan for RAM	1. Write a verification plan for RAM? (C3)
Unit 4: Assertions	
Assertions for a given RAM using system verilog	1. Experiment assertions for given RAM using System Verilog (C4)
Unit 5: Testbench Infrastructure:	
Verification environment for memory	1. Experiment verification environment for Memory.(C4)
Unit 6: Stimulus and Response	
Randomization technique	1. Experiment randomization technique for Memory in System Verilog. (C4)
Unit 7: Coverage-Driven Verification	
Verification environment for RAM	1. Develop verification environment for RAM.
Unit 8: Assertions for Formal Tools	
Equivalence check for RAM	1. Model linting, equivalence check for RAM using cadence (C4)
Unit 9: System-Level Verification	
Verification environment for MIPS	1. Develop verification environment for MIPS processor (C6)
Unit 10: Processor Integration Verification	
Verification environment for MIPS	1. Develop verification environment for MIPS processor(C6)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-

Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4
Sessional Examination 1	*	*		
Sessional Examination 2			*	*
Assignment/Presentation				*
Laboratory examination	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Janick Bergeron, Verification methodology manual for SystemVerilog, Springer. 2. Janick Bergeron, Writing Testbenches using System Verilog, Springer.

	3. William K. Lam, Hardware Design Verification - Simulation and Formal Method Based Approaches. 4. Pallab Dasgupta, A Roadmap for Formal Property Verification, Springer.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	**System on Chip Lab**
Course Code: EDA-608L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:** Basic knowledge of Computer Architecture, C programming language

Synopsis:	This Course provides insight on 1. The concept of C++ for SystemC 2. The concept of SystemC for hardware descriptions as a netlist 3. The concept of systems approach towards electronic system level flow 4. The concept of SystemC for data processing, data storage, communications and control mechanisms
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe the hardware in terms of input, output with sub blocks
CO 2:	Apply the basics of VLSI design on the problem statements
CO 3:	Examine the correctness of the design

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*				*					
CO 2	*	*			*						
CO 3		*					*				

Course content and outcomes:

Content	***Competencies***
Unit 1:	
Introduction to System Approach	1. Describe SystemC for hardware description languages (C2)

Unit 2:	
Electronic System Level Flow	1. Apply SystemC for FSM based system (C3)
Unit 3:	
Design Principles in SOC Architecture	1. Apply SystemC for RISC Architecture (C3)
Unit 4:	
Processors	1. Examine SystemC for MIPS/ARM Processor (C4)
Unit 5:	
Memory Design	1. Examine SystemC for memory based design (C4)
Unit 6:	
Hardware/Software Interfaces	1. Examine SystemC for PHY Layer of USB/Ethernet/PCIe (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation			*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• IEEE Standard for Standard SystemC® Language Reference Manual by IEEE Computer Society • SystemC: From the Ground Up by David C. Black, Jack Donovan, Bill Bunton, Anna Keist

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	CAD for VLSI Lab
Course Code: EDA-609L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:** Basics of Data structures, Graph theory, VLSI CAD algorithms, C programming.

Synopsis:	This Course provides insights on : 1. Representation of circuits using data structures 2. Implementation of VLSI CAD algorithms 3. Develop parts of EDA tools used in VLSI Design automation
Course Outcomes (COs):	On successful completion of this course, students will be able to :
CO 1:	Illustrate a given circuit in the form of a suitable graph using data structures
CO 2:	Experiment VLSI CAD algorithms using C and data structures
CO 3:	Design building blocks of EDA tools

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*	*								
CO 3				*	*						

Course content and outcomes:

Content	***Competencies***
Unit 1:	
Layout Compaction, Placement and Partitioning Floor planning:	At the end of the topic students should be able to: 1. Experiment placement algorithms (C4) 2. Experiment floor planning algorithms (C4)

Floor planning concepts, Shape Functions and Floor plan sizing Routing: Global routing, algorithms for global routing, local routing, types of local routing problems	3. Experiment global and local routing algorithms C4)
Unit 2:	
Area Routing, algorithms for area routing, Channel routing, algorithms for channel routing. Logic synthesis and verification High level logic synthesis: Need for high-level logic synthesis, Design representation and Transformation	1. Experiment area routing algorithms (C4) 2. Experiment channel routing algorithms (C4) 3. Experiment logic synthesis algorithms (C4)
Unit 3 :	
Partitioning Scheduling Allocation	1. Experiment partitioning algorithms (C4) 2. Experiment scheduling algorithms (C4) 3. Experiment allocation algorithms (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-

Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*		
Sessional Examination 2		*	*
Assignment/Presentation		*	*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Graph theory" , Narsingh Deo (Prentice-Hall of India private ltd) 2. "Graph theory" , Gibbons 3. "Algorithms for VLSI Design Automation" , Sabih H. Gerez (John Wiley and Sons)

	4. "High Level Synthesis -Introduction to chip and System Design" , Daniel Gajski, Nikil Dutt, Allen Wu, Steve Lin (Kluwer Academic Publishers) 5. "Logic synthesis and verification algorithms" , Gary D. Hachtel, Fabio Somenzi (Kluwer Academic Publishers)

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(Deemed to be University under Section 3 of the UGC Act, 1956)

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	**Digital Signal Processing Lab**
Course Code: ESD-603L	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:** Knowledge of Signals and Systems and Basic Knowledge of Matlab

Synopsis:

This Course provides insight on

1. Understanding of basics of Signal and Systems as pre-requisite.
2. Understanding the concepts of Fast Fourier Transforms.
3. Learning hardware implementation of systems.
4. Learning FIR and IIR Filter Designs.
5. Learning concepts of multi-rate signal processing in the form of sampling rate conversion, structures of sampling rate converters and some applications of sampling rate converters
6. Understanding three optimum Weiner filters, adaptive algorithm and transforming Weiner filters in to adaptive filters
7. Understanding architecture, memory management and pipelining concepts of TMS320C67XX processor through self-stud.

Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Use matlab to implement various DSP techniques. (C3)
CO 2:	Experiment DFT, LTI techniques and analyse the results. (C4)
CO 3:	Design FIR, Butterworth and Chebychev filters in matlab. (C5)

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*		*	*						
CO 2	*	*			*						
CO 3	*	*		*	*						

Course content and outcomes:

Content	*Competencies*
Unit 1:	
Write matlab programs to Generate waves Write matlab programs to Addition of two sequences Write matlab programs to Find convolution of two sequences and verify the result using built-in function User defined Matlab function to find convolution of two sequences and verify the result	Use Matlab to generate waves.(C3) Use Matlab for addition of two sequences.(C3) Compute convolution of two sequences using Matlab. (C3) Analyse the convolution usinf built in functions. (C4) Practice convolution user defined function in Matlab (C3)
Unit 2:	
Write matlab programs to Find DTFT of a sequence. Write matlab programs to Find DFT of a sequence and verify using built-in function User defined Matlab function to find DFT and verify the result Write matlab programs to Find convolution of two sequences using DFT Write matlab programs to Find the time response of an LTI system defined by either difference equation or transfer function	Experiment DTFT of a sequence using Matlab (C4) Analyse the DFT of a sequence with built in function (C4) Experiment DFT using Matlab (C4) Compute convolution of two sequence using DFT in Matlab. (C3) Experiment time response of an LTI system in Matlab (C4)
Unit 3:	

Write Matlab programs to find DFT using DIT-FFT and DIF-FFT algorithms, compare the result using built in function. Design FIR filters with frequency domain specification (LP, HP, BP and BR) using Frequency Sampling Technique and verify frequency response. Design FIR filter to meet required impulse response using Frequency Sampling Technique.	Analyse DIT-FFT and DIF-FFT algorithms. (C4) Design FIR filters with frequency domain specifications. (C5)
Unit 4:	
Write Matlab programs to Design FIR filters with frequency domain specification (LP, HP, BP and BR) using different window functions and verify frequency response. Design analog Butterworth and Chebychev filters using built-in functions, transform them to digital filter and verify their frequency response (C2). Design digital Butterworth and Chebychev filters using built-in functions verify the frequency response (C2)	Design FIR filters with frequency domain specifications. (C5) Design analog Butterworth and Chebychev filters using built-in functions. (C5) Design digital Butterworth and Chebychev filters using built-in functions. (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-

Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Assignment/Presentation			*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• "Digital Signal Processing", Sanjith K Mitra • "Digital Signal Processing", Oppenheim and Schafer • "Digital Signal Processing", Roman Kuc • "Digital Signal Processing", Proakis and Manolakis • "Digital Signal Processing ", Rabinder and Gold • Shaum Out-Line Series

	• "Signals and Systems", Symon Haykins • DSP Processors and Fundamentals • "Multirate signal processing", Vaidyanathan • "Handbook of DSP", Elliot

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Mini Project - 1
Course Code: EDA 695	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester1
No of Credits: 4	**Prerequisites:** Any programming language and circuit basics

Synopsis:	Students are expected to select a problem in the area of their interest and the area of their specialization that would require an implementation in hardware / software or both in a semester
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Apply the objectives of the project work and provide an adequate background with a detailed literature survey
CO 2:	Breakdown the project into sub blocks with sufficient details to allow the work to be reproduced by an independent researcher
CO 3:	Compose hardware/software design, algorithms, flowchart, methodology, and block diagram
CO 4:	Evaluate the results
CO 5:	Summarize the work carried out

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1				*							
CO 2					*			*			
CO 3							*			*	
CO 4						*					*
CO5:							*				

Course content and outcomes:

Content	***Competencies***
Phase 1	

Problem identification, synopsis submission, status submission, mid evaluation.	At the end of the topic student should be able to: 1. Identify the problem/specification (C1) 2. Discuss the project (C2) 3. Prepare the outline (C3) 4. Describe the status of the project (C2) 5. Prepare a mid-term project presentation report (C3) 6. Prepare and present mid-term project presentation slides (C3, C5) 7. Develop project implementation in hardware/software or both in chosen platform (C5)
Phase 2	
Status submission, final evaluation.	1. Prepare the progress report (C3) 2. Prepare the final project presentation report (C3) 3. Prepare and present final project presentation slides (C3, C5) 4. Modify and Develop implementation in hardware/software or both in chosen platform (C3, C5) 5. Justify the methods used and obtained results (C6)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	-	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	48	-

Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-
Practical	-	-
Revision	-	-
Assessment	03	-
TOTAL	**51**	**09**

Assessment Methods:

Formative:	**Summative:**
Project Problem Selection	Mid-Term Presentation
Synopsys review	Second status review
First status review	Demo & Final Presentation

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Mid Presentation	*	*			
Presentation	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	Particular to the chosen project

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Seminar - 1
Course Code: EDA 697	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 1
No of Credits: 1	**Prerequisites:** Communication Skill
Synopsis:	1. To select, search and learn technical literature. 2. To Identify a current and relevant research topic. 3. To prepare a topic and deliver a presentation. 4. To develop the skill to write a technical report. 5. Develop ability to work in groups to review and modify technical content.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Show competence in identifying relevant information, defining and explaining topics under discussion.
CO 2:	Show competence in working with a methodology, structuring their oral work, and synthesizing information.
CO 3:	Use appropriate registers and vocabulary, and will demonstrate command of voice modulation, voice projection, and pacing.
CO 4:	Demonstrate that they have paid close attention to what others say and can respond constructively.
CO 5:	Develop persuasive speech, present information in a compelling, well-structured, and logical sequence, respond respectfully to opposing ideas, show depth of knowledge of complex subjects, and develop their ability to synthesize, evaluate and reflect on information.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1											
CO 2											
CO 3											

CO 4											
CO5:											

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	-	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	14	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-
Practical	-	-
Revision	-	-
Assessment	-	-
TOTAL	**14**	**-**

Assessment Methods:

Formative:	**Summative:**
Seminar Topic Selection	
Synopsys review	
PPT Review	

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Presentation	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	Particular to the chosen Seminar

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Advanced VLSI Design
Course Code: EDA 604	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:**

Synopsis:	This Course provides insight on
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	To learn modelling, analysis, and design of analog circuits using CMOS technologies.
CO 2:	Introduce the principles of analog circuits and apply the techniques for the design of CMOS analog integrated circuits.
CO 3:	Apply the methods learned in the class to design and implement practical projects

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*								
CO 2		*	*								
CO 3	*	*							*		

Course content and outcomes:

Content	***Competencies***
Unit 1: CMOS passive elements	
Resistor: Fabrication – Different layers used, Layout techniques and practical considerations, Temperature and voltage dependence resistors, Active resistors – advantages	1. Design Layout of passive components in CMOS technology (C5)

Capacitor: Fabrication – "poly-substrate", "poly-poly", "metal-poly" – comparison, Layout techniques, Temperature and voltage dependence, Active Capacitors.	
Unit 2: Analog MOSFET Models	
Low frequency MOSFET Model: Small-signal model of the MOSFET in saturation, Derivation for gm and r_0 High frequency MOSFET Model: Variation of transconductance with frequency	1. Develop analog MOSFET model (C5)
Unit 3: Current Sources and Sinks	
Current Source, current Sink and Current Mirror – Differences, Applications ,Current Mirror-Basic current mirror, The cascode current mirror – advantages, derivation ,for o/p resistance r0,Layout of current Sources/Sinks/Mirrors, Matching in MOSFET mirrors, Other Current Sources /Sinks/Mirrors- Wilson current mirror, Regulated cascode current mirror	1. Design current sources and sinks for a given specification (C5)
Unit 4: References	
Voltage Dividers, Sensitivity and Fractional temperature coefficients-Resistor-MOSFET divider, MOSFET-only voltage divider, Current Source Self-	1. Design voltage and current references and to make them insensitive to voltage and temperature variation (C5)

Biasing-Threshold voltage referenced self biasing, Diode referenced self biasing,Thermal voltage referenced self biasing, Bandgap voltage references, Bandgap referenced biasing, Beta Multiplier Referenced Self-Biasing-A voltage reference, Operation in the Sub threshold region	
Unit 5: CMOS Single Stage Amplifiers	
Amplification – need for amplification, basic concepts, Important performance parameters – "Analog Design Octagon" ,Common Source (CS) Amplifier-Derivation for Av and comparison of CS Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Drain Amplifier (or Source Follower)-Derivation for Av and comparison of CD Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - Common Gate Amplifier-Derivation for Av and comparison of CG Amplifier with: Passive resistor load, MOSFET/Diode-Connected/ /Active load, Current source load - The Push-Pull Amplifier, Noise and Distortion in Amplifiers-A	1. Design CMOS single stage amplifier for a given specification (C5)

class AB Amplifier - Modelling Amplifier Noise	
Unit 6: Differential Amplifiers	
The Source Coupled Pair-Current Source Load, Common-Mode Rejection Ratio, Noise, Matching Considerations. The Source Cross-Coupled Pair-Current Source Load Cascode Loads, Wide-Swing Differential Amplifiers, Current Differential Amplifier, Constant Transconductance Diff-Amp.	1. Design and simulate differential amplifier for a given specification with different types of load (C5)
Unit 7: Frequency Response of Amplifiers	
Introduction, Frequency response of single stage amplifiers, Frequency response of Differential pair.	1. Design and test frequency response of single stage amplifier (C5)
Unit 8: Noise	
Statistical characteristics of noise, types of noise, representation of noise in circuits, noise in single-stage amplifiers, noise in differential pairs, noise bandwidth.	1. Illustrate various types of noise affects amplifier operation (C4)
Unit 9: Operational Amplifiers	
Basic CMOS Op-Amp Design-Characterizing the op-Amp, Compensating the Op-amp Without Buffer, The Cascode Input Op-amp, Operational Transconductance Amplifiers.	1. Illustrate basic design of operational amplifier and OTA. (C4)
Unit 10: Nonlinear Analog Circuits	
Design of Basic CMOS Comparator, Characterizing the Comparator - Adaptive	1. Design of nonlinear analog circuits (C5)

Biasing, Analog Multipliers-The Multiplying Quad, Level Shifting, Multiplier Design Using Squaring Circuits.	
Unit 10: Dynamic Analog Circuits	
The MOSFET Switch - Switched-Capacitor Integrator Circuits	1. Illustrate switched capacity circuits (C4)
Unit 10: Data Converter Fundamentals and Architectures	
Sample-and-Hold (S\H) Characteristics, DAC and ADC Specifications, Architectures – Cyclic DAC, Pipeline DAC, Pipeline ADC, Integrating ADCs, SAR ADC	1. Design of various types of ADC and DAC (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos			
Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation		*	*
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "CMOS Circuit Design, Layout, and Simulation", Baker, Li, & Boyce, IEEE Press, 1998. 2. " Design of Analog CMOS Integrated Circuits", Razavi, McGraw-Hill, Inc., 2000. 3. "Analog Integrated Circuit Design ", Johns & Martin, , John Wiley & Sons, 1997. 4. "CMOS Analog Design, 2nd Ed." ,Allen & Holberg, Oxford Univ. Press, 1987. 5. " Analysis and Design of Analog Integrated Circuits ",Gray & Meyer, John Wiley & Sons, 1984. 6. "Analog VLSI" ,Mohammed Ismail, & Terri Fiez, , McGraw-Hill, Inc. 7. "VLSI - Design Techniques for Analog and Digital Circuits",Geiger, Allen, & Strader McGraw-Hill, Inc., 8. Recent papers from IEEE Journal of Solid state Circuits and other technical magazines

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Low Power VLSI Design
Course Code: EDA 605	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** CMOS circuit fundamentals, Digital and Analog circuits

Synopsis:	This Course provides insights on 1. Various components of power dissipation in CMOS 2. Fundamentals of various approaches to low power design 3. Low power design techniques 4. Design of low power building blocks
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe various components of power in CMOS VLSI Design
CO 2:	Comprehend various leakage power reduction techniques, technology and scaling related aspects of low power VLSI design
CO 3:	Explain low power design methodologies and flows
CO 4:	Apply low power techniques for designing VLSI building blocks

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*	*								
CO 3			*								
CO 4				*	*						

Course content and outcomes:

Content	***Competencies***
Unit 1: Overview of power dissipation in CMOS	

Dynamic and Static power components, Leakage current components, Factors affecting leakage power, Examples	1. Illustrate of basics of low power design (C3) 2. Describe various power dissipation components in CMOS technology (C2)
Unit 2: Circuit techniques for leakage power reduction:	
Circuit techniques for leakage power reduction: Stacking – natural and artificial, Multiple Vth techniques - Multiple Channel Doping's, Multiple Oxide CMOS (MOXCMOS) Circuits, Multiple Channel Lengths, Multiple Body Biases, Multi-threshold-voltage CMOS (MTCMOS), Dual Threshold CMOS, Variable Threshold CMOS (VTMOS), Dynamic Threshold CMOS (DTMOS), Dynamic Vth techniques – Vth hopping scheme, Dynamic voltage scaling(DVTS) scheme.	1. Illustrate of various circuit techniques of leakage power reduction (C3) 2. Illustrate basics of dynamic power reduction (C3) 3. Describe various dynamic V_{th} techniques (C2)
Unit 3: Technology scaling for dynamic power reduction	
Scaling techniques – constant voltage, constant field and lateral scaling.	1. Illustrate scaling techniques (C3)
Unit 4: Voltage scaling approaches	
Reliability-Driven Voltage Scaling, Technology-Driven Voltage Scaling, Energy x Delay Minimum Based Voltage Scaling, Voltage Scaling through Optimal Transistor Sizing, Voltage Scaling using Threshold Reduction, Architecture-Driven Voltage Scaling.	1. Describe different voltage scaling approaches for dynamic power reduction (C2)

Unit 5: Glitch power	
Generated and propagated glitches, Glitch power analysis, Reduction techniques, Gate triggering approach.	Illustrate significance of glitch power and techniques to reduce the same (C3)
Unit 6: Clock gating	
Principle, Combinational and sequential clock gating, Clock gating efficiency.	Illustrate clock gating principle and its types and techniques (C3)
Unit 7: Adiabatic techniques for low power	
Adiabatic techniques for low power	Illustrate adiabatic techniques for low power design (C3)
Unit 8: Logic optimization for low power, Power modelling, Power analysis	
Logic optimization for low power, Power modelling, Power analysis	Describe various design tool level support to low power VLSI design (C2)
Unit 9: System level issues in multi-voltage designs, Level shifters	
System level issues in multi-voltage designs, Level shifters	Illustrate low power design issues at system level (C3)
Unit 10: Low power design of building blocks	
Low power design of building blocks	Apply low power design techniques to design VLSI building blocks (C3)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-

TOTAL	44	74

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation		*	*
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Low-Power CMOS VLSI Circuit Design",Kaushik Roy and Sharat C. Prasad, Wiley-Interscience. 2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995. 3. "Low Power Design Methodologies",J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996. 4. "Low – Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996. 5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998. 6. "Logic synthesis for Low – power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998. 7. "Power Aware Design Methodologies", Pedram, Massoud, Rabaey, Jan M., Kluwer Academic Publishers.

	8. "Low-power Digital Systems Based on Adiabatic- Switching Principles", W.C. Athas, L. Swensson, J.G. Koller and E. Chou, , IEEE Transactions on VLSI Systems, vol. 2, pp. 398-407, December 1994. 9. "A survey of power estimation techniques in VLSI circuits", F. Najm, IEEE Transactions on VLSI Systems, vol. 2, pp. 446-455, December 1994.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Universal Verification Methodology
Course Code: EDA 606	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:**

Synopsis:	This Course provides insight on 1. To study the basic structure of UVM. 2. To understand UVM library basics. 3. To Study the basic concepts of OOPs. 4. To understand the different components of verification environment. 5. To understand the concept of Register Abstraction Layer, TLM Communications.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Model a scenario for Verification of a DUT in UVM.
CO 2:	Analyse the usefulness of a driver, monitor, checker, test cases in UVM verification environment.
CO 3:	Explain component configuration and factory.
CO 4:	Explain the concept of Register Abstraction Layer and TLM communications.
CO 5:	Design test bench to verify the functionality of a design.
Co 6:	Design a VIP for an IP as a project.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1		*									
CO 2		*									
CO 3	*										
CO 4	*										
CO 5			*								

CO 6			*								

Course content and outcomes:

Content	***Competencies***
Unit 1: UVM overview	
Verification Planning and Coverage-Driven Verification, Multi-Language and Methodologies. UVM Testbench and environments, Interface UVCs, System and Module UVCs, the System Verilog UVM class library.	1. Explain UVM testbench and environments. (C2) 2. Explain System Verilog UVM class library. (C2)
Unit 2: Object Oriented Programming	
Introduction, What is an object in OOP, Distributed development environment, Classes, Objects, Programs, Using generalization and inheritance, polymorphism in OOP, Downcast, Class libraries, Static methods and attributes, parameterized classes, packages and namespaces.	1. Explain polymorphism, inheritance, encapsulation and abstraction. (C2) 2. Explain static methods and parameterized classes. (C2)
Unit 3: UVM library basics	
Using UVM library, Library Base Classes, the uvm_object class, the uvm_component class, UVM configuration mechanism, TLM in UVM, UVM factory, UVM message facilities, callbacks.	1. Explain uvm_component and uvm_object class. (C2) 2. Explain TLM in UVM (C2) 3. Explain UVM factory and callbacks (C2)
Unit 4: Interface UVCs	
Stimulus modeling and generation, creating the driver, creating the sequencer, connecting the driver	1. Explain stimulus modelling and generation in UVM (C2)

and sequencer .	2. Explain the creation of driver, sequencer and connecting them. (C2)
Unit 5:	
Creating the collector and monitor, modeling topology with UVM, creating the Agent, creating the UVM verification component, creating UVM sequences, configuring the sequencer's default sequence, coordinating end-of-test, implementing protocol-specific coverage and checks, handling reset, packaging interface UVCs.	1. Explain how to create UVM sequences. (C2) 2. Explain the concept of packaging interface UVCs. (C2)
Unit 6: Component Configuration and Factory	
Establish and Query Component Parent-Child Relationships, Set Up Component Virtual SystemVerilog Interfaces with uvm_config_db, Constructing Components and Transactions with UVM Factory, Implement Tests to Configure Components, Implement Tests to Override Components with Modified Behaviour.	1. Explain the concept of factory and component configuration (C2)
Unit 7: UVM Callback	
Create User Callback Hooks in Component Methods, Implement Error Injection with User Defined Callbacks, Implement Component Functional Coverage with User Defined Callbacks, Review Default Callbacks in UVM Base Class.	1. Explain the concept of UVM callback. (C2)
Unit 8: Simple Testbench integration	

Testbenches and Tests, creating a simple testbench, testbench configuration, creating a test, creating meaningful tests, virtual sequencers and sequences, checking for DUT correctness, implementing a coverage model.	1. Explain steps to creating simple testbench. (C2) 2. Describe virtual sequencers and sequences. (C1) 3. Explain how to implement coverage model. (C6)
Unit 9: Stimulus generation topics	
Fine control sequence generation, executing multiple sequences concurrently, using p_sequencer, using pre_body() and post_body() methods, controlling the arbitration of items, interrupt sequences, protocol layering.	1. Explain the concept of fine control sequence generation and executing multiple sequences concurrently. (C2)
Unit 10: Register Abstraction Layer	
Registers, Specification, Adapter, Integrating, Integration, Register Model Overview, Model Structure, Quirky Registers, Model Coverage, Back Door Access, Generation, Stimulus Abstraction, Memory Stimulus, Sequence Examples, Built in Sequences, Scoreboarding, Functional Coverage.	1. Explain register model overview, adapter, model structure quirky registers and back door access. (C2)
Unit 11: System UVCs and Testbench Integration	
Introduction, module and system UVC architecture, sub-components of module and system UVCs, module UVC configuration, the testbench, sequences, coverage, stand-In mode, scalability	1. Explain scalability concerns in system verification. (C2)

concerns in system verification, module UVC Directory structure.	
Unit 12: TLM Communications	
TLM Push, Pull and Fifo Modes, TLM Analysis Ports, TLM Pass-Through Ports, TLM 2.0 Blocking and Non-Blocking Transport Sockets	1. Explain TLM push, pop, fifo, TLM analysis ports, blocking and non-blocking transport sockets. (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6
Sessional Examination 1	*	*				
Sessional Examination 2			*	*	*	
Assignment/Presentation						*

End Semester Examination	*	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Sharon Rosenberg, Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Lulu publishers, 2010. 2. Vanessa R. Cooper, "Getting started with UVM: A beginner's guide", Verilab publisher, 2013. 3. UVM Cookbook, Verification Academy, 2013. 4. UVM User's guide, Accellera, 2011.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Scripting for VLSI
Course Code: EDA 607	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:**

Synopsis:	The goal of the course is to 1. Study of scripting languages such as Bash and Perl in Linux environment. 2. The study of usage of scripting languages in VLSI field. 3. To provide the basic knowledge about different tools available to automate the task
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1	Discover shell script programmatically using different features and debugging the code
CO 2	Apply SED & AWK commands to do more complex task in easy way
CO 3	Apply PERL scripts that create and change scalar, array and hash variables

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*	*								
CO 2	*	*		*							
CO 3		*	*	*							

Course content and outcomes:

Content	***Competencies***
Unit 1: Essentials	
Structure of a Linux Based Operating System, Hardware, Kernel, files & file system; Processes; networking; version control.	1. Summarize the Structure of a Linux Based Operating System 2. Discuss Hardware, Kernel (C2) 3. Explain files & file system, Processes; networking; version control(C2)

Unit 2: Introduction to Scripting: Shell, Tcl/tk, perl, python	
Shell Programming: Variables; User defined variables (UDV); Rules for Naming variable name; echo Command; Shell Arithmetic; Quotes; Exit Status; Wild cards; Command Line arguments; Redirection of Standard output/input; Pipes; Filter; shell language constructs.	1. Explain Variables, User defined variables (UDV) (C2) 2. Examine the Rules for Naming variable name (C3) 3. Write basic shell script using echo Command, Shell Arithmetic, Quotes, Exit Status, Wild cards, Command Line arguments; Redirection, Pipes, constructs. (C3)
Unit 3: Awk utility	
Awk utility	1. Illustrate Data manipulation using awk utility(C3) 2. Experiment Regular expression using awk utility (C4) 3. Experiment script using conditional statement using awk (C4)
Unit 4: Sed & Make	
cut utility; paste utility; join utility; tr utility; Data manipulation using awk utility, sed utility; uniq utility, grep utility; Make Utility.	1. Illustrate File operations using sed operations (C3) 2. Write the importance of make utility (C2) 3. Construct make utility (C5)
Unit 5: Perl	
Introduction to Perl; Unary operator; Binary Operators; Statements; Constructs.	1. Experiment Perl program using Perl constructs (C4)
Unit 6: Pattern Matching Subroutines	
Pattern Matching Subroutines; formats; References; Packages.	1. Illustrate Pattern matching (C3) 2. Discover Generate formats (C3)
Unit 7: Modules; overloading	
Modules; overloading	1. Illustrate Importance of modules (C3)

	2. Experiment overloading (C4)
Unit 8:	
Unicode; Interprocess; threads; compiling; command line interface.	**1.** Constructs Perl one liners (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation			*
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Introduction to Linux – A Beginner's Guide", Machtelt Garrels 2. "Unix shell programming", Stephen G. Kochan, Patrick H. Wood 3. "Sed & awk ",Dale Dougherty, Arnold Robbins 4. "Programming Perl", Larry Wall, Tom Christiansen, Jon Orwant

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	IT Project Management
Course Code: CSE 631	**Course Instructor:**
Academic Year: 2020 – 2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** Familiarity in developing application using any high level language

Synopsis:	This Course provides insight on 1. The concept of software development process and project management 2. Illustrates the difference between a lab assignment and group project 3. Help the students to understand the finer points of Project management 4. Bring awareness about the processes, tools and techniques involved in the field of IT project management
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Illustrate the importance of project planning.
CO 2:	Discuss and demonstrate various tools applicable for different phases of the software project.
CO 3:	Illustrate the importance of Change management.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*									
CO 2		*	*								
CO 3	*		*								

Course content and outcomes:

Content	***Competencies***
Unit 1: Software Project Planning	
Understand the Project Needs, Create the Project Plan, Diagnosing Project Planning Problems	1. Understand the project needs, necessity of plan, Define the Project Plan, Diagnosing Project Planning Problems (C1)

Unit 2: Estimation	
Elements of a Successful Estimate, Wideband Delphi Estimation, Other Estimation Techniques, Diagnosing Estimation Problems.	1. List the importance of estimation and describe different estimation techniques (C2) 2. Discuss the significance of Reviews and different review techniques (C2)
Unit 3: Project Schedules	
Building the Project Schedule, Managing Multiple Projects, Use the Schedule to Manage Commitments, Diagnosing Scheduling Problems.	1. Outline the steps in building project schedule.(C1) 2. Indicate mechanism of managing multiple projects. (C2)
Unit 4: Reviews	
Inspections, Deskchecks, Walkthroughs, Code Reviews, Pair Programming, Use Inspections to Manage Commitments, Diagnosing Review Problems.	1. Discuss the significance of Reviews and different review techniques (C2)
Unit 5: Software Requirements	
Requirements Elicitation, Use Cases, Software Requirements Specification, Change Control, Introduce Software Requirements Carefully, Diagnosing Software Requirements Problems	1. Introduce to requirement elicitation techniques, design and demonstrate the requirement documentation by field visits(C2)
Unit 6 : Design and Programming	
Review the Design, Version Control with Subversion, Refactoring, Unit Testing, Use Automation, Be Careful with Existing Projects, Diagnosing Design and Programming Problems	1. Illustrate the key steps in design and programming phase. Version control and unit testing significance (C3)

Unit 7: Software Testing	
Test Plans and Test Cases, Test Execution, Defect Tracking and Triage, Test Environment and Performance Testing, Smoke Tests, Test Automation, Postmortem Reports, Using Software Testing Effectively, Diagnosing Software Testing Problems	1. Define the test plans, significance of test phase and the test case characteristics. Introduce different types testing and significance of type of testing.(C2)
Unit 8: Understanding Change	
Why Change Fails, How to Make Change Succeed	1. Illustrate the necessity of Change management system – developing impact analysis document and its importance (C3).
Unit 9: Management and Leadership	
Take Responsibility, Do Everything Out in the Open, Manage the Organization, Manage Your Team	1. Understand the role of management in motivating the team, finer points of managing the team (C2)
Unit 10: Managing an Outsourced Project	
Prevent Major Sources of Project Failure, Management Issues in Outsourced Projects, Collaborate with the Vendor	1. Describe the differences of managing the outsourced project, typical point of conflicts(C2) 2. Review of the project management process (C2)
Unit 10: Process Improvement	
Life Without a Software Process, Software Process Improvement, Moving Forward	**1.** Analyse the projects without process and continuous process improvements initiatives needed for success of the project (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60

Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2	*		*
Assignment/Presentation	*	*	
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Applied Software Project Management" By Jennifer Greene, Andrew Stellman (O'Reilly Publications) 2005. 2. "The Art of Project Management" By Scott Berkun (O'Reilly Publications) 2005.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Physical Design
Course Code: EDA-610	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** Basic knowledge of digital design

Synopsis:	This Course provides insight on 1. This course provides the concept of CMOS circuit and layout design 2. This course provides the knowledge of floor planning, placement, clock tree synthesis, and routing 3. This course provides the concept of parasitic extraction of layout 4. This course provides the knowledge testing in VLSI Design 5. This course provides the concept of fault modelling and fault simulation 6. This course provides the knowledge of DFT and BIST in VLSI design
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe CMOS logic gate design, identify physical design of simple gates, give examples logic structures
CO 2:	Explain procedure involved in floorplan step, placement, clock tree synthesis, routing, and extraction of layout
CO 3:	Classify digital testing, give examples of fault modelling and fault simulation, test single stuck at faults, describe design for testability, ad-hoc DFT, scan based designs, built-in self-test

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*								
CO 2	*	*									
CO 3		*	*								

Course content and outcomes:

Content	*Competencies*
Unit 1: CMOS circuit and layout design	
CMOS logic gate design- Basic physical design of simple gates - CMOS logic structures - Clocking strategies	1. Recall CMOS structure (C1) 2. Describe logic gate design (C2) 3. Give examples of physical design of combinational circuit (C2) 4. Explain clocking strategies (C2)
Unit 2: Floorplan	
Floorplan .	1. Explain technology file (C2) 2. Describe different formats of circuit description 3. Explain design constraints (C2) 4. Explain the design planning, clock planning and power planning (C2) 5. Describe macro placement (C2)
Unit 3: Placement	
Placement.	1. Define standard cells in ASIC design (C1) 2. Describe standard cell mapping onto ASIC components (C2) 3. Estimate core area and standard cell placement region (C6)
Unit 4: Clock tree synthesis	
Clock tree synthesis	1. Explain clock tree algorithms (C2)
Unit 5: Routing	
Routing.	1. Explain special routing algorithms (C2) 2. Describe special routing algorithms (C2) 3. Explain detail routing algorithms (C2)
Unit 6: RC extraction	
RC extraction.	1. Describe extraction procedure (C2) 2. Summarize the physical design flow (C6)

Unit 7: Back annotation	
Back annotation	1. Summarize the physical design flow (C6)
Unit 8: Testing	
Introduction to Digital Testing - Fault modeling - Fault Simulation - Testing for Single stuck faults - Design For Testability (DFT) - Ad-Hoc DFT - Scan based designs - Built-In Self-Test (BIST)	1. Differentiate verification and testing (C2) 2. Explain test concerns (C2) 3. Describe fault modelling and simulation (C2) 4. Explain ATE architecture and instrumentation (C2) 5. Explain and give examples of stuck at faults (C2) 6. Describe making circuits testable (C2) 7. Describe testability insertion (C2) 8. Explain testability of combinational and sequential circuits (C2) 9. Explain memory based BIST, differentiate BIST types (C2) 10. Describe test pattern generation (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos			
Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*		
Sessional Examination 2		*	*
Assignment/Presentation	*		
End Semester Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Neil H. E. Weste, David Harris, Kamran Eshraghian, "Principles of CMOS VLSI Design: A systems perspective", Third Edition, Addison Wesley,2008 2. Majid Sarrafzadeh, C. K. Wong , "An introduction to VLSI physical design", McGraw Hill, 1996, ISBN 0070571945, 9780070571945, 334 pages 3. Khosrow Golshan, "Physical design essentials: an ASIC design implementation perspective", Springer, 2007, ISBN 0387366423, 9780387366425, 211 pages 4. Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, "Nano-CMOS circuit and physical design", John Wiley and Sons, 2004, ISBN 0471466107, 9780471466109, 393 pages

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Advanced Logic Synthesis
Course Code: EDA-611	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** Concepts of Digital Design

Synopsis:	This Course provides insight on • This course provides the concept of logic synthesis of combinational circuits • This course provides the concept of logic synthesis of sequential circuits • This course provides the concept of technology mapping
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe logic synthesis process
CO 2:	Explain procedure involved in logic synthesis of combinational and sequential circuits
CO 3:	Classify multilevel logic synthesis and technology mapping

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*									
CO 3			*								

Course content and outcomes:

Content	***Competencies***
Unit 1: Introduction to logic synthesis	
Introduction to logic synthesis	1. Recall sets and relations(C1) 2. Describe Boolean function (C2)
Unit 2: Two-level logic synthesis	
Introduction Boolean algebra concepts	1. Explain Boolean algebra concepts (C2) 2. Solve combinational circuit problems using k-map (C3)

Minimization using k-map Minimization using Tabular method Consensus theorem Iterative Consensus theorem Recursive computation Unate covering problem a) Reduction technique b) MIS algorithm c) Branch and bound algorithm	3. Explain Tabular method, Iterative Consensus theorem, Recursive computation, and Unate covering problem (C2) 4. Solve problems on Tabular method, Iterative Consensus theorem, Recursive computation, and Unate covering problem (C3)
Unit 3: Sequential logic synthesis	
Introduction Basics of FSM concept Minimization of completely specified FSM a) Equivalent partition algorithm Minimization of Incompletely specified FSM a) Compatible table b) Maximum compatibles c) Prime compatibles d) Binate covering problem FSM traversal algorithms a) Depth first search b) Breadth first search c) Shortest path	1. Explain concept of FSM (C2) 2. Explain concept of completely specified FSM (C2) 3. Solve completely specified FSM problems using equivalent partition algorithm (C3) 4. Explain Incompletely specified FSM (C2) 5. Solve problems using Compatible table, Maximum compatibles, Prime compatibles, Binate covering problem (C3) 6. Explain FSM traversal algorithms (C2)

State encoding and optimization	
Unit 4: Multilevel logic synthesis	
Introduction Algebraic and Boolean Division Kernels and Cokernels Algebraic and Boolean resubtitution methods	1. Describe multi-level logic synthesis with networks and algebraic operations (C2) 2. Reproduce switching functions in factored form (C1) 3. Explain division with Kernels and Co-Kernels (C2) 4. Explain decomposition and restructuring (C2) 5. Solve problems using above algorithms (C3)
Unit 5: Technology mapping	
a) Graph covering and Technology mapping b) Tree covering by Dynamic programming c) Decomposition d) Delay optimization and Graph covering	1. Describe graph covering and technology mapping (C2) 2. Describe DAG-Covering problem (C2) 3. Explain delay optimization and graph covering (C2)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	36	72
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-

Practical	36	72
Revision	-	-
Assessment	6	-
TOTAL	**78**	**144**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*		
Sessional Examination 2		*	*
Assignment/Presentation		*	
End Semester Examination	*	*	*
Laboratory examination			

Feedback Process	• End-Semester Feedback
Reference Material	1. "Logic Synthesis and Verification Algorithms",Gary D. Hachtel and Fabio Somenzi (Kluwer Academic Publishers) 2. "Logic Minimization Algorithms For VLSI Synthesis" ,Robert K. Brayton ,Gary D. Hachtel, Curtis T. McMullen and Alberto L. Sangiovanni-Vincentelli (Kluwer Academic Publishers)

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Wireless Communications and Antenna Design
Course Code: EDA-613	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** Basic knowledge of electronics and communication

Synopsis:	This course provides insight on • Wireless communication system and evolution of different systems and standards • Recent wireless communication technologies used for communication • Architecture, functioning, protocols, capabilities and application of various wireless communication networks • Design, types, functioning, and applications of antennas
Course Outcomes (COs):	At the end of the course student shall be able to
CO 1:	Describe wireless communication systems and different wireless communication standards
CO 2:	Identify various wireless communication technologies
CO 3:	Explain the architecture, functioning, protocols, capabilities and application of various wireless communication networks.
CO 4:	Demonstrate multiple access techniques for wireless communication
CO 5:	Explain design of antennas including types, functioning, and applications

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*									
CO 3			*								

CO 4				*							
CO 5				*							

Course content and outcomes:

Content	***Competencies***
Unit 1: Introduction	
Definition of wireless communication, various generations and standards in cellular communication system	1. Define wireless communication (C1) 2. Describe three different generations of wireless communication (C2) 3. Illustrate GPS, wireless local loop, cordless phone, paging systems, and RFID (C3)
Unit 2: Modern wireless technologies	
The concept of satellite, wireless networking, WIMAX, Wi-Fi, and Bluetooth technology, the concept of types of wireless data transmission	1. Relate concept of satellite, wireless networking, WIMAX, Wi-Fi, and Bluetooth technology (C4). 2. Study Wireless Router, Wireless Adapters, Wireless Repeater, Microwave, Infrared (C3) 3. Study the types of Wireless Devices, Radio, Wireless Phones, Advantages and Disadvantages of Wireless Communications (C3)
Unit 3: Wireless and Cellular Communication	
Multiple access techniques in wireless communication	1. Study Simplex, Half Duplex and Full Duplex communication modes and Multiple Access Options: Frequency, Time or Code (C1) 2. Describe Frequency Division Multiple Access, Time Division Multiple Access,

	Spatial Division Multiple Access, Beam Division Multiple Access (BDMA), Code Division Multiple Access (C2) 3. Explain Frequency Reuse, Channel Assignment, Handoff, Cell Splitting, Cell Sectoring, Micro Zone Method (C2)
Unit 4: Wireless personal area networks	
Define wireless personal area networks, and different communication standards	1. Compare Bluetooth, UWB and ZigBee modes of communication (C4) 2. Describe IEEE 802.11, network architecture, medium access methods, WLAN standards (C2)
Unit 5: Ad-hoc wireless networks	
Design Challenges in Ad-hoc wireless networks, concept of cross layer design, security in wireless networks, energy constrained networks	1. Define Ad-hoc wireless networks (C1) 2. Explain cross layer design and security in wireless networks (C2) 3. Describe mobile network layer protocol (C2)
Unit 6: Antenna design	
Properties of Antennas, Radiation Structures, Arrays, Dipoles, Slots, and Loops	1. Describe antennas (C1) 2. Explain Antennas for Various Applications (C2) 3. Describe Dipole, Monopole, Loop and Slot Antennas, Linear and Planar Arrays, Microstrip Antennas, Helical Antennas, Horn Antennas, Reflector Antennas (C1)
Learning strategies, contact hours and student learning time	

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Sessional Examination 1	*	*			
Sessional Examination 2			*	*	
Assignment/Presentation	*	*	*	*	
End Semester Examination	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Andrea Goldsmith, "Wireless Communications", Cambridge University Press, 2005.

	2. Sanjay Kumar, "Wireless Communication the Fundamental and Advanced Concepts" River Publishers, Denmark, 2015 (Indian reprint). 3. Vijay K Garg, "Wireless Communications and Networks", Morgan Kaufmann Publishers an Imprint of Elsevier, USA 2009 (Indian reprint) 4. J. Schiller, "Mobile Communication" 2/e, Pearson Education, 2012. 5. Iti Saha Misra, "Wireless Communication and Networks : 3G and Beyond", 2/e, McGraw Hill Education (india) Private Ltd, New Delhi, 2013. 6. C.A. Balanis, Antenna Theory – Analysis and Design, John Wiley, 2005 7. J.D. Kraus and R.J. Marhefka, Antennas, McGraw Hill, 2003

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Machine learning for VLSI Design
Course Code: EDA-614	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:** Basic Programming
Synopsis:	This course provides insight on • Machine learning, applications, techniques, design issues and approaches to machine learning • Fundamental knowledge about concept learning, hypothesis and bias • Neurons and biological motivation, activation functions and threshold units, supervised and unsupervised learning, perceptron network models in Artificial Neural Networks • Learning from unclassified data using clustering techniques • Support Vector Machines for linear and non-linear classification • Deep Learning and Reinforcement Learning algorithms • Application of machine learning for VLSI design steps
Course Outcomes (COs):	At the end of the course student shall be able to
CO 1:	Identify the goals, applications, types and design issues of machine learning techniques.
CO 2:	Describe activation functions, weights and threshold units used in artificial neural networks, supervised and unsupervised learning, gradient descent approach, types of perceptron models, overfitting
CO 3:	Demonstrate artificial neural network models, clustering models, support vector classifier models, Deep learning models and reinforcement learning models
CO 4:	Design back propagation neural network, K-means and agglomerative clustering, deep neural network, reinforcement learning models and selection of a machine learning algorithm for the given data analysis.
CO 5:	Describe machine learning for VLSI design steps

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*									
CO 3			*								
CO 4				*							
CO 5				*							

Course content and outcomes:

Content	***Competencies***
Unit 1: Introduction	
Definition of Machine Learning, Goals and applications of machine learning, Basic design issues and approaches to machine learning, Types of machine learning techniques	1. Define Machine Learning (C1) 2. Describe about any three applications for which machine learning approaches seem appropriate. (C2) 3. Illustrate different types of machine learning techniques (C3)
Unit 2: Inductive Classification	
The concept learning task, Concept learning as search through a hypothesis space, General-to-specific ordering of hypotheses, Finding maximally specific hypotheses, Version spaces and the candidate elimination algorithm, Inductive bias.	1. Relate concept learning and hypothesis space (C4). 2. Apply different algorithms to obtain most general and most specific hypotheses from the training examples. (C3)
Unit 3: Decision Tree learning	
Representing concepts as decision trees, Recursive induction of decision trees, Picking the best splitting	1. Apply decision tree algorithm to find the hypothesis space (C3)

attribute, Entropy and information gain, Searching for simple trees and computational complexity.	2. Construct decision tree machine learning algorithm (C5) 3. Explain the method of choosing training examples and target function in the design of a machine learning system (C2) 4. Explain different validation technique to find the accuracy in training and testing of data set (C5)
Unit 4: Bayesian learning	
Probability theory and Bayes rule, Naive Bayes learning algorithm - Parameter smoothing, Generative vs. discriminative training, Logistic regression, Bayes nets and Markov nets for representing dependencies	1. Write the applications of Bayes theorem (C3) 2. Describe the use of Logistic Regression in Machine Learning (C2) 3. Predict the target value for the new instance using Naïve Bayes classifier. (C3)
Unit 5: Artificial Neural Networks	
Neurons and biological motivation, Activation functions and threshold units, Supervised and unsupervised learning, Perceptron Model: representational limitation and gradient descent training, Multilayer networks and back propagation, Overfitting	1. Relate biological neurons with artificial neurons and the motivation for ANN development. (C1) 2. Distinguish Supervised and unsupervised learning (C2). 3. Describe about error reduction techniques in used Artificial Neural Networks based learning (C2) 4. Write the usability of different activation functions for ANN learning system. (C3) 5. Describe the architecture of various perceptron networks. (C2)
Unit 6: Clustering	

Learning from unclassified data, Clustering. Hierarchical Agglomerative Clustering, Non- Hierarchical Clustering - k-means partitional clustering, Expectation maximization (EM) for soft clustering, Semi-supervised learning with EM using labelled and unlabelled data.	1. Write the different methods of learning from unclassified data (C3). 2. Explain the operations of various clustering models in machine learning (C5) 3. Describe the methods used for measuring dissimilarity between two clusters. (C2) 4. Apply clustering techniques for data analysis. (C3)
Unit 7: Support Vector Machines, Deep Learning and Reinforcement Learning	
Introduction to Deep Learning, Introduction to convolutional Neural Network (CNN), CNN Architecture and layers, N-arm Bandit Problem, Calculating the Value Function, Associative Learning	1. Define Deep Learning. (C1) 2. Describe the applications of deep learning. (C2) 3. Explain the architecture of Deep Neural Network and CNN (C5) 4. Explain the concept of Multi-Armed Bandit Problem (MABP). (C2) 5. Outline the learning process and characteristics of reinforcement learning
Unit 8: Machine Learning in VLSI Design	
Taxonomy, Machine Learning for Lithographic Process Models, Masks, and Physical Design, Yield Enhancements, Machine Learning based Aging Analysis, Energy-Efficient Design of Advanced Machine Learning Hardware	1. Describe Machine Learning steps for fabrication steps (C1) 2. Explain aging analysis using machine learning approach (C2) 3. Describe energy-efficient systems based on machine learning (C1)
Learning strategies, contact hours and student learning time	

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Sessional Examination 1	*	*			
Sessional Examination 2			*	*	
Assignment/Presentation	*	*	*	*	
End Semester Examination	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Bishop, C. (2006). Pattern Recognition and Machine Learning. Berlin: Springer-Verlag. 2. Ethem Alpaydin, Introduction to Machine Learning, PHI

	3. Trevor Hastie, Robert Tibshirani, Jerome Friedman, The Elements of Statistical Learning Data Mining,Inference,and Prediction 4. Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, eds. Machine Learning in VLSI Computer-Aided Design. Springer, 2019.

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(Deemed to be University under Section 3 of the UGC Act, 1956)

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Entrepreneurship
Course Code: ENP-601	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 3	**Prerequisites:**

Synopsis:	This course introduces students to the theory of entrepreneurship and its practical implementation. It focuses on different stages related to the entrepreneurial process, including business model innovation, monetization, small business management as well as strategies that improve performance of new business ventures. Centered on a mixture of theoretical exploration as well as case studies of real-world examples and guest lectures, students will develop an understanding of successes, opportunities and risks of entrepreneurship. This course has an interdisciplinary approach and is therefore open to students from other Majors.
Course Outcomes (COs):	On successful completion of this course, students will be able to:
CO 1:	To impart knowledge on the basics of entrepreneurial skills and competencies to provide the participants with necessary inputs for creation of new ventures.
CO 2:	To familiarize the participants with the concept and overview of entrepreneurship with a view to enhance entrepreneurial talent
CO 3:	To appraise the entrepreneurial process starting with pre-venture stage
CO 4:	To Create and exploit innovative business ideas and market opportunities
CO 5:	To Build a mind-set focusing on developing novel and unique approaches to market opportunities
CO 6:	To explore new vistas of entrepreneurship in 21st century environment to generate innovative business ideas through case studies.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2				*							
CO 3			*								
CO 4						*					

CO 5								*			
CO 6										*	

Course content and outcomes:

Content	*Competencies*
Unit 1: Introduction to Entrepreneurship	
Meaning and Definition of Entrepreneurship-Employment vs Entrepreneurship, Theories of Entrepreneurship, approach to entrepreneurship, Entrepreneurs VS Manager	1. Explain the meaning of Entrepreneurship (C1) 2. Discuss the theories of Entrepreneurship (C1) 3. Discuss the approaches to Entrepreneurship (C1)
Unit 2: Entrepreneurial Traits	
Personality of an entrepreneur, Types of Entrepreneurs	1. Discuss the Personality traits of entrepreneurs. (C2)
Unit 3: Process of Entrepreneurship	
Factors affecting Entrepreneurship process	1. Identify the fundamentals and responsibilities of entrepreneurship (C2) 2. Exemplify one's capabilities in relation to the rigors of successful ventures (C3) 3. Identify and differentiates the different characteristics and competencies of an entrepreneurs (C2)
Unit 4: Business Start-up Process	
Idea Generation, Scanning the Environment, Macro and Micro analysis	1. Explain the Process of Business start up (C1) 2. Develop creativity and critical thinking in identifying opportunities (C5) 3. Apply innovative approaches in envisioning ones entrepreneurial career (C3)
Unit 5: Business Plan writing	
Points to be considered, Model Business plan	1. Identify different business models (C3) 2. Describe different parts of a business plan(C2)

Unit 6: Case studies	
Indian and International Entrepreneurship	1. Perform self-assessment and analyse entrepreneurial personal traits and competencies (C4) 2. Evaluate oneself and plan courses of action to help develop one's entrepreneurial characteristics and competencies. (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	30	60
Quiz	02	04
Small Group Discussion (SGD)	02	02
Self-directed learning (SDL)	-	04
Problem Based Learning (PBL)	02	04
Case Based Learning (CBL)	-	-
Revision	02	-
Assessment	06	-
TOTAL	**44**	**74**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5	CO 6
Sessional Examination 1	*	*				
Sessional Examination 2			*	*		
Assignment/Presentation					*	*

End Semester Examination	*	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. NVR Naidu and T. Krishna Rao, "Management and Entrepreneurship", IK International Publishing House Pvt. Ltd 2008. 2. Mohanthy Sangram Keshari, "Fundamentals of Entrepreneurship", PHI Publications, 2005 3. Butler, D. (2006). Enterprise planning and development. USA: Elsevier Ltd. Gerber, M.E. (2008) Awakening the entrepreneur within. NY: Harper Collins.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Advanced VLSI Design Lab
Course Code: EDA 604L	**Course Instructor**
Academic Year: 2019-2020	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic Electronics, Digital Systems
Synopsis:	This Course provides insight on
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	design and test simple basic building blocks of CMOS analog circuits at the transistor level, including mask layout
CO 2:	Get hands-on in design and simulate CMOS integrated circuits using Computer Aided Design (CAD) Tools.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*			*							
CO 2		*			*	*					

Course content and outcomes:

Content	***Competencies***
Unit 1: CMOS passive elements	
1. To design CMOS layouts for resistors and capacitors and simulate their behaviour.	1. design CMOS layouts for resistors and capacitors (C5)
Unit 2: Analog MOSFET Models	
To draw MOSFET models for various circuit configurations and practice	1. Model MOSFET for various circuit configurations (C4)

Unit 3: Current Sources and Sinks	
Design, simulate and verify current mirror circuits for different current and voltage specifications.	1. Design and verify current mirror circuit (C5)
Unit 4: References	
Design, simulate and verify different types of voltage and current reference circuits for different currents and voltages.	1. Design and verify different current reference circuits for different currents and voltages. (C5)
Unit 5: CMOS Single Stage Amplifiers	
Design, simulate and verify Common Source, Common Gate, Common Drain single stage CMOS amplifiers with different types of loads.	1. Design and verify Common Source, Common Gate, Common Drain single stage CMOS amplifiers with different types of loads.(C5)
Unit 6: Differential Amplifiers	
Design, simulate and verify a simple differential amplifier with passive resistor, current mirror and current source loads.	1. Design and verify a simple differential amplifier with passive resistor.(C5)
Unit 7: Noise	
Simulate and carryout noise analysis of simple amplifier circuits and plot noise characteristics.	1. Design noise analysis of simple amplifier circuits.(C5)
Unit 8: Operational Amplifiers	
Design, simulate and verify a simple 2-stage Operational amplifier	1. Design and verify a simple 2-stage Operational amplifier .(C5)

Unit 9: Nonlinear Analog Circuits	
Design, simulate and verify a few important nonlinear analog circuits	1. Design and verify nonlinear analog circuits.(C5)
Unit 10: Dynamic Analog Circuits	
Design, simulate and verify simple switched capacitor circuits	1. Design and verify simple switched capacitor circuits.(C5)
Unit 11: Data Converter Fundamentals and Architectures	
Design, simulate and verify a few DAC and ADC circuits	1. Design and verify a few DAC and ADC circuits .(C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination

Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2
Sessional Examination 1	*	*
Sessional Examination 2	*	*
Assignment/Presentation	*	*
End Semester Examination	*	*
Laboratory examination	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Cadence user manual

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Low Power VLSI Design Lab
Course Code: EDA 605L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic understanding of Low power VLSI Design, Digital, and Analog circuit basics, familiarity with Spice simulation

Synopsis:	This Course provides insight on : 1. Various power components of CMOS circuits 2. Circuit techniques for static power reduction 3. Circuit techniques for dynamic power reduction 4. Design of low power building blocks
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Design circuits to reduce static power
CO 2:	Implement dynamic power reduction techniques
CO 3:	Apply low power techniques to design low power circuits

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2		*	*								
CO 3				*	*						

Course content and outcomes:

Content	***Competencies***
Unit 1:	
Introduction to Low Power Design, Overview of power dissipation in CMOS: Dynamic and Static power	At the end of the topic students should be able to :

components, Leakage current components, Circuit techniques for leakage power reduction	1. Experiment CMOS digital blocks and find various power dissipation components(C4) 2. Apply leakage reduction techniques to sample gates and flip-flops (C3)
Unit 2:	
Technology scaling for dynamic power reduction Voltage scaling approaches Glitch power, Cock gating Adiabatic techniques for low power	1. Design a digital module and implement voltage scaling technique for power reduction.(C5) 2. Experiment clock gating for power reduction for the above module(C4)
Unit 3:	
Logic optimization for low power System level issues in multi-voltage designs Low power design of building blocks	1. Design basic digital VLSI modules using low power techniques (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-

Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*		
Sessional Examination 2		*	*
Assignment/Presentation			*
Laboratory Examination		*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Low-Power CMOS VLSI Circuit Design",Kaushik Roy and Sharat C. Prasad, Wiley-Interscience. 2. "CMOS Low Power Digital Design", A. Chandrakasan & R. Brodersen, Kluwer Academic Pubs. 1995. 3. "Low Power Design Methodologies",J. Rabaey & M. Pedram, , Kluwer Academic Pubs. 1996. 4. "Low – Power Digital VLSI Design, Circuits and Systems", Bellaour & M.I. Elamstry ,Kluwer Academic Publishers, 1996. 5. S. Imam & M. Pedram, Kluwer Academic Publishers, 1998.

	6. "Logic synthesis for Low – power VLSI Designs", B.G.K.Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Publishers, 1998.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Universal Verification Methodology Lab
Course Code: EDA 606	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:**

Synopsis:	This Course provides insight on 1. To study the basic structure of UVM. 2. To understand UVM library basics. 3. To Study the basic concepts of OOPs. 4. To understand the different components of verification environment. 5. To understand the concept of Register Abstraction Layer, TLM Communications.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Model a scenario for Verification of a DUT in UVM.
CO 2:	Implement a driver, monitor, checker, test cases in UVM verification environment.
CO 3:	Implement Register Abstraction Layer and TLM communications.
CO 4:	Design test bench to verify the functionality of a design.
CO 5:	Design a VIP for an IP as a project.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*		*								
CO 2	*				*						
CO 3		*			*						
CO 4	*		*								
CO 5	*		*								

Course content and outcomes:

Content	*Competencies*
Unit 1: UVM overview	
UVM overview	1. Practice UVM packages and libraries in project environment (C3)
Unit 2: Object Oriented Programming	
Object Oriented Programming	1. Experiment inheritance, polymorphism, abstraction and encapsulation using System Verilog in UVM. (C4)
Unit 3: UVM library basics	
UVM library basics	1. Experiment driver, sequencer and connect driver and sequencer. (C4)
Unit 4: Interface UVCs	
Interface UVCs	1. Experiment monitor and collector, UVM sequences. (C4)
Unit 5: Component Configuration and Factory	
Component Configuration and Factory	1. Practice Component Virtual System Verilog Interfaces with uvm_config_db. (C3)
Unit 6: UVM Callback	
VM Callback	1. Constructing Components and Transactions with UVM Factory.
Unit 7: Simple Testbench integration	
Simple Testbench integration	1. Experiment Tests to Configure Components (C4)
Unit 8: Stimulus generation topics	

Stimulus generation topics	1. Experiment Tests to Override Components with Modified Behaviour.(C4)
Unit 9: Register Abstraction Layer	
Register Abstraction Layer	1. Experiment Component Functional Coverage with User Defined Callbacks. (C4)
Unit 10: System UVCs and Testbench Integration	
System UVCs and Testbench Integration	1. Design verification environment for RAM.(C5)
Unit 11: TLM Communications	
TLM Communications	1. Design verification environment for MIPS processor (C5)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Sessional Examination 1	*	*			
Sessional Examination 2			*	*	
Assignment/Presentation					*
Laboratory examination	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Sharon Rosenberg, Kathleen Meade, "A Practical Guide to Adopting the Universal Verification Methodology (UVM)", Lulu publishers, 2010. 2. Vanessa R. Cooper, "Getting started with UVM: A beginner's guide", Verilab publisher, 2013. 3. UVM Cookbook, Verification Academy, 2013. 4. UVM User's guide, Accellera, 2011.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Scripting for VLSI Lab
Course Code: EDA 607L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year Semester 2
No of Credits: 1	**Prerequisites:** Problem solving, basic programming

Synopsis:	This Course provides insight on 1. Study of scripting languages such as Bash and Perl in Linux environment. 2. The study of usage of scripting languages in VLSI field. 3. To provide the basic knowledge about different tools available to automate the task
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Experiment shell script programmatically using different features and debugging the code
CO 2:	Operate SED & AWK commands to do more complex task in easy way
CO 3:	Experiment PERL scripts that create and change scalar, array and hash variables

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*										
CO 2			*								
CO 3	*				*						

Course content and outcomes:

Content	***Competencies***
Unit 1:	

Essentials	1. Understand the basic concepts of shell, kernel, operating system (C2). 2. Able to create user account (c3)
Unit 2:	
Introduction to Scripting: Shell, Tcl/tk, perl, python	1. Able to write shell script and debug the script (C3) 2. Understand the importance of shell script in real wold. (C2)
Unit 3:	
Awk utility	1. Generate report using awk script (C3)
Unit 4:	
Sed & Make	1. Perform file handling function using sed script (C4) 2. Appraise the importance of MAKE file (C3)
Unit 5:	
Perl	1. Create pattern matching , report generation and perform file handling function using Perl Script (C3)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-

Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	36	-
Revision	-	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation	*	*	
Laboratory examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Introduction to Linux – A Beginner's Guide", Machtelt Garrels 2. "Unix shell programming", Stephen G. Kochan, Patrick H. Wood 3. "Sed & awk ",Dale Dougherty, Arnold Robbins "Programming Perl", Larry Wall, Tom Christiansen, Jon Orwant

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	**IT Project Management Lab**
Course Code: CSE-631L	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Familiarity in developing application using any high level language

Synopsis:	This Course provides insight on 1. The concept of software development process and project management 2. Illustrates the difference between a lab assignment and group project 3. Help the students to understand the finer points of Project management 4. Bring awareness about the processes, tools and techniques involved in the field of IT project management.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Practice the project development through project planning.
CO 2:	Understand the finer points of Project management.
CO 3:	Bring awareness about the processes, tools and techniques involved in the field of IT project management.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1			*	*							
CO 2					*				*		
CO 3			*		*						

Course content and outcomes:

Content	*Competencies*
Unit 1: Software Project Planning	
Understand the Project Needs, Create the Project Plan, Diagnosing Project Planning Problems.	1. Discussion on tools needed for project management (C3)
Unit 2: Estimation	
Elements of a Successful Estimate, Wideband Delphi Estimation, Other Estimation Techniques, Diagnosing Estimation Problems.	1. Download and demonstrate the tools typically used for UML design. (C3)
Unit 3: Project Schedules	
Building the Project Schedule, Managing Multiple Projects, Use the Schedule to Manage Commitments, Diagnosing Scheduling Problems.	1. Design the application through the UML tool practiced (C4) 2. Develop the team with different roles assigned to each member – namely project manager, developer, tester and assign appropriate tasks (C4)
Unit 4: Reviews	
Inspections, Deskchecks, Walkthroughs, Code Reviews, Pair Programming, Use Inspections to Manage Commitments, Diagnosing Review Problems.	1. Develop basic set of programs and to illustrate the unit tests (C2)
Unit 5: Software Requirements	
Requirements Elicitation, Use Cases, Software Requirements Specification, Change Control, Introduce Software	1. Field visit to develop and practice the requirement elicitation (C3)

Requirements Carefully, Diagnosing Software Requirements Problems	
Unit 6: Design and Programming	
Review the Design, Version Control with Subversion, Refactoring, Unit Testing, Use Automation, Be Careful with Existing Projects, Diagnosing Design and Programming Problems	1. Illustrate the key steps in design and programming phase. Version control and unit testing significance (C3) 2. Review of various artefacts generated by project and revise the project management methodology to the team (C5)
Unit 7: Software Testing	
Test Plans and Test Cases, Test Execution, Defect Tracking and Triage, Test Environment and Performance Testing, Smoke Tests, Test Automation, Postmortem Reports, Using Software Testing Effectively, Diagnosing Software Testing Problems	1. Inter team testing set up based on requirement document(C5)
Unit 8: Understanding Change	
Why Change Fails, How to Make Change Succeed	1. Illustrate the necessity of Change management system – SVN hands on (C3).
Unit 9: Management and Leadership	
Take Responsibility, Do Everything Out in the Open, Manage the Organization, Manage Your Team	1. Discussion on the topic with the help of case study (C3)
Unit 10: Managing an Outsourced Project	
Prevent Major Sources of Project Failure, Management Issues in	2. Discussion on the topic with the help of case study (C3)

Outsourced Projects, Collaborate with the Vendor	
Unit 11: Process Improvement	
Life Without a Software Process, Software Process Improvement, Moving Forward	1. Post-mortem report generation of respective project by each team – review of the report and suggest areas of improvement (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos			
Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2			*
Assignment/Presentation	*		
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. "Applied Software Project Management" By Jennifer Greene, Andrew Stellman (O'Reilly Publications) 2005. 2. "The Art of Project Management" By Scott Berkun (O'Reilly Publications) 2005.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Physical Design Lab
Course Code: EDA-610L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic knowledge of digital design, Verilog HDL

Synopsis:	This Course provides insight on 1. The concept of generating netlist from the hardware description language 2. The concept of CAD tools for generating layout of a digital design 3. The concept of verifying the generated layout of a digital design
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe the floorplan, placement and routing of a digital design
CO 2:	Apply the RC extraction procedure and back annotation for the layout
CO 3:	Examine the correctness of the generation of layout by simulation

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*				*					
CO 2	*				*						
CO 3		*	*				*				

Course content and outcomes:

Content	***Competencies***
Unit 1:	
Introduction to logic synthesis - 1	Describe synthesis and placement tools for digital design implementation (C2)
Unit 2:	

Introduction to logic synthesis - 2	Apply HDL to generate netlist with the design library and constraints (C3)
Unit 3:	
Placement, Routing and Extraction	Use CAD tools to perform placement, routing, and extraction (C3)
Unit 4:	
Back annotation	Examine the correctness of the implementation using design rule check, layout versus schematic check and simulation procedure (C4)
Unit 5:	
Physical Synthesis - 1	Developing the physical design and synthesis for digital combinational designs (C4)
Unit 6:	
Physical Synthesis - 2	Developing the physical design and synthesis for digital sequential designs (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:	
Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos			
Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2		*	*
Assignment/Presentation			*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• IEEE Standard for Standard SystemC® Language Reference Manual by IEEE Computer Society • SystemC: From the Ground Up by David C. Black, Jack Donovan, Bill Bunton, Anna Keist

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Advanced Logic Synthesis Lab
Course Code: EDA-611L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic knowledge of digital design, Verilog HDL

Synopsis:	This Course provides insight on 1. The concept of generating netlist from the hardware description language 2. The use of CAD tools for generating netlist from a digital design 3. The concept of netlist simulation with timing delay information
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe the library and constraint files required for synthesis of a digital design
CO 2:	Apply the CAD tools for generating the netlist
CO 3:	Examine the timing, power, and area reports after the synthesis along with simulation

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*	*				*					
CO 2	*		*		*						
CO 3	*		*								

Course content and outcomes:

Content	***Competencies***
Unit 1:	

Introduction to CAD tools for logic synthesis - 1	Describe synthesis process synthesis tools for digital design implementation (C2)
Unit 2:	
Introduction to logic synthesis - 2	Apply HDL to generate netlist with the design library and constraints (C3)
Unit 3:	
Synthesis of combinational circuits	Use CAD tools to perform synthesis of digital combinational circuits (C3)
Unit 4:	
Synthesis of sequential circuits	Use CAD tools to perform synthesis of digital sequential circuits (C3)
Unit 5:	
Synthesis verification - 1	Examine the correctness of the implementation using netlist generation and reports generated for constraints of combinational circuits (C4)
Unit 6:	
Synthesis verification - 2	Examine the correctness of the implementation using netlist generation and reports generated for constraints of sequential circuits (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-

Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1		*	*
Assignment/Presentation		*	*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• Switching and Finite Automata Theory by Zvi Kohavi and Niraj K. Jha • IEEE Standard Verilog® Hardware Description Language by IEEE Computer Society

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Wireless Communications and Antenna Design Lab
Course Code: EDA-613L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basic knowledge of programming

Synopsis:	This course provides insight on The concept of wireless communication The concept of digital modulation and modulation domain analysis The concept of effects of filters in wireless communication systems and investigation of various pulse shaping filters and wireless channel and channel impact in wireless communication
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Describe Matlab for wireless communication
CO 2:	Apply Matlab for digital modulation and modulation domain analysis
CO 3:	Examine effects of filters and channel impact in wireless communication

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1						*					
CO 2					*						
CO 3							*				

Course content and outcomes:

Content	***Competencies***
Unit 1:	

Introduction to Matlab Toolbox and Simulink	Describe Matlab tools for wireless communication (C2)
Unit 2:	
Introduction to RF system-level simulation of wireless transceivers - 1	Apply Model and Simulate for Wireless Systems (C3)
Unit 3:	
Wireless transceivers - 1	Use Matlab tools to design and implement wireless transceivers (C3)
Unit 4:	
Wireless transceivers - 2	Examine simulation for correctness of wireless transceivers (C3)
Unit 5:	
Design of Zigbee receiver - 1	Use Matlab tools to implement Zigbee receiver (C3)
Unit 6:	
Design of Zigbee receiver - 2	Examine simulation for correctness receivers (C3)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-

Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Assignment/Presentation			*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	• Garg, V., 2010. Wireless communications & networking. Elsevier. • Cho, Y.S., Kim, J., Yang, W.Y. and Kang, C.G., 2010. MIMO-OFDM wireless communications with MATLAB. John Wiley & Sons.

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Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Machine Learning for VLSI Design Lab
Course Code: EDA-614L	**Course Instructor:**
Academic Year: 2020-2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:** Basics of Programming
Synopsis:	This course provides insight on • Machine learning, applications, techniques, design issues and approaches to machine learning • Fundamental knowledge about concept learning, hypothesis and bias
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Identify the software and tools for designing machine-learning applications.
CO 2:	Apply concept learning and hypothesis space.
CO 3:	Demonstrate Artificial Neural Network, Clustering, Support Vector Machine, Deep Neural Network and Reinforcement Learning models, Support Vector Machine

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1						*					
CO 2					*						
CO 3							*				

Course content and outcomes:

Content	***Competencies***
Unit 1:	
Goals and applications of machine learning	1. Identify programming environments available for the machine learning (C1)

Basic design issues and approaches to machine learning	2. Classify the pros and cons of various environments for ML coding (C2)
Unit 2:	
The concept learning task. Concept learning as search through a hypothesis space. General-to-specific ordering of hypotheses.	1. Design a machine learning model to get a Maximally Specific Hypothesis for the given training examples (C5). 2. Construct a machine learning model to obtain most general and most specific hypotheses for the given training examples (C5)
Unit 3:	
Probability theory and Bayes rule. Naive Bayes learning algorithm - Parameter smoothing. Logistic regression. Bayes nets and Markov nets for representing dependencies	1. Design a machine learning model using Bayes learning (C5). 2. Develop a machine learning classifier models using different approach (C5) 3. Design Bayes nets and Markov nets for representing dependencies (C5)
Unit 4:	
Neurons and biological motivation. Activation functions and threshold units. Supervised and unsupervised learning Perceptron Model: representational limitation and gradient descent training.	1. Demonstrate activation functions, weights and threshold units in artificial neural networks (C3) 2. Demonstrate ANN models (C3) 3. Design of ANN models for classification (C5) 4. Analyse the performance issues (C4)

Multilayer networks and back propagation. Overfitting.	
Unit 5:	
Learning from unclassified data. Clustering. Hierarchical Aglomerative Clustering. Non-Hierarchical Clustering - k-means partitional clustering. Expectation maximization (EM) for soft clustering. Semi-supervised learning with EM using labeled and unlabled data.	1. Demonstrate various clustering models in machine learning (C3) 2. Design different types of clusters (C5) 3. Analyse the performance of clustering techniques on different data (C4) 4. Apply clustering techniques for data analysis. (C3)
Unit 6:	
Maximum margin linear separators. Quadractic programming solution to finding maximum margin separators. Kernels for learning non-linear functions. Varying length pattern classification using SVM	1. Demonstrate Maximum margin linear separators. (C3) 2. Design SVM classifiers (C5) 3. Analyse the performance of SVM (C4)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-

Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Assignment/Presentation			*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	1. Machine Learning, T. Mitchell, McGraw-Hill, 1997 2. Machine Learning, E. Alpaydin, MIT Press, 2010 3. Machine Learning for Big Data, Jason Bell, Wiley Big Data Series

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Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Entrepreneurship Lab
Course Code: ENP-601L	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 1	**Prerequisites:**

Synopsis:	This Course provides insight on This course introduces students to the theory of entrepreneurship and its practical implementation. It focuses on different stages related to the entrepreneurial process, including business model innovation, monetization, small business management as well as strategies that improve performance of new business ventures. Cantered on a mixture of theoretical exploration as well as case studies of real-world examples and guest lectures, students will develop an understanding of successes, opportunities and risks of entrepreneurship. This course has an interdisciplinary approach and is therefore open to students from other Majors.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Understand the concept of entrepreneurship
CO 2:	To appraise the entrepreneurial process starting with pre-venture stage through group discussion
CO 3:	To Build a mind-set focusing on developing novel and unique approaches to market opportunities by considering case studies and understand the complete flow of entrepreneurship

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*					*		*			
CO 2						*					
CO 3								*		*	

Course content and outcomes:

Content	*Competencies*
Unit 1: Introduction to Entrepreneurship	
Meaning and Definition of Entrepreneurship-Employment vs Entrepreneurship, Theories of Entrepreneurship, approach to entrepreneurship, Entrepreneurs VS Manager	1. Discuss the theories of Entrepreneurship (C1) 2. Discuss the approaches to Entrepreneurship (C1)
Unit 2: Process of Entrepreneurship	
Factors affecting Entrepreneurship process	1. Exemplify one's capabilities in relation to the rigors of successful ventures (C3) 2. Identify and differentiates the different characteristics and competencies of an entrepreneurs (C2)
Unit 3: Business Plan writing	
Points to be considered, Model Business plan	1. Identify different business models (C3) Describe different parts of a business plan(C2)
Unit 4: Case studies	
Indian and International Entrepreneurship	1. Perform self-assessment and analyse entrepreneurial personal traits and competencies (C4) 2. Evaluate oneself and plan courses of action to help develop one's entrepreneurial characteristics and competencies. (C5)
Learning strategies, contact hours and student learning time	

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	12	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	03	-
Clinic	-	-
Practical	24	-
Revision	03	-
Assessment	06	-
TOTAL	**48**	**-**

Assessment Methods:

Formative:	**Summative:**
Internal practical Test	Sessional examination
Theory Assignments	End semester examination
Lab Assignment & Viva	Viva

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3
Sessional Examination 1	*	*	
Sessional Examination 2			*
Assignment/Presentation		*	*
Laboratory Examination	*	*	*

Feedback Process	• End-Semester Feedback

Reference Material	1. NVR Naidu and T. Krishna Rao, "Management and Entrepreneurship", IK International Publishing House Pvt. Ltd 2008. 2. Mohanthy Sangram Keshari, "Fundamentals of Entrepreneurship", PHI Publications, 2005 3. Butler, D. (2006). Enterprise planning and development. USA: Elsevier Ltd. Gerber, M.E. (2008) Awakening the entrepreneur within. NY: Harper Collins.

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Mini Project - 2
Course Code: EDA 696	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester 2
No of Credits: 4	**Prerequisites:** Any programming language and circuit basics

Synopsis:	Students are expected to select a problem in the area of their interest and the area of their specialization that would require an implementation in hardware / software or both in a semester
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Apply the objectives of the project work and provide an adequate background with a detailed literature survey
CO 2:	Breakdown the project into sub blocks with sufficient details to allow the work to be reproduced by an independent researcher
CO 3:	Compose hardware/software design, algorithms, flowchart, methodology, and block diagram
CO 4:	Evaluate the results
CO 5:	Summarize the work carried out

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1				*							
CO 2					*			*			
CO 3							*			*	
CO 4						*					*
CO5:							*				

Course content and outcomes:

Content	***Competencies***
Phase 1	

Problem identification, synopsis submission, status submission, mid evaluation.	At the end of the topic student should be able to: 1. Identify the problem/specification (C1) 2. Discuss the project (C2) 3. Prepare the outline (C3) 4. Describe the status of the project (C2) 5. Prepare a mid-term project presentation report (C3) 6. Prepare and present mid-term project presentation slides (C3, C5) 7. Develop project implementation in hardware/software or both in chosen platform (C5)
Phase 2	
Status submission, final evaluation.	1. Prepare the progress report (C3) 2. Prepare the final project presentation report (C3) 3. Prepare and present final project presentation slides (C3, C5) 4. Modify and Develop implementation in hardware/software or both in chosen platform (C3, C5) 5. Justify the methods used and obtained results (C6)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	-	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	48	-

Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-
Practical	-	-
Revision	-	-
Assessment	03	-
TOTAL	**51**	**09**

Assessment Methods:

Formative:	**Summative:**
Project Problem Selection	Mid-Term Presentation
Synopsys review	Second status review
First status review	Demo & Final Presentation

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Mid Presentation	*	*			
Presentation	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	Particular to the chosen project

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Seminar - 2
Course Code: EDA 698	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** First Year, Semester2
No of Credits: 1	**Prerequisites:** Communication Skill
Synopsis:	1. To select, search and learn technical literature. 2. To Identify a current and relevant research topic. 3. To prepare a topic and deliver a presentation. 4. To develop the skill to write a technical report. 5. Develop ability to work in groups to review and modify technical content.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	Show competence in identifying relevant information, defining and explaining topics under discussion.
CO 2:	Show competence in working with a methodology, structuring their oral work, and synthesizing information.
CO 3:	Use appropriate registers and vocabulary, and will demonstrate command of voice modulation, voice projection, and pacing.
CO 4:	Demonstrate that they have paid close attention to what others say and can respond constructively.
CO 5:	Develop persuasive speech, present information in a compelling, well-structured, and logical sequence, respond respectfully to opposing ideas, show depth of knowledge of complex subjects, and develop their ability to synthesize, evaluate and reflect on information.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1	*							*	*		*
CO 2	*							*	*		*
CO 3	*							*	*		*

CO 4	*							*	*		*
CO5:	*							*	*		*

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	-	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	14	-
Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-
Practical	-	-
Revision	-	-
Assessment	-	-
TOTAL	**14**	**-**

Assessment Methods:

Formative:	**Summative:**
Seminar Topic Selection	
Synopsys review	
PPT Review	

Mapping of assessment with Cos

Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Presentation	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	Particular to the chosen Seminar

Name of the Program:	Master of Engineering (ME) – VLSI Design
Course Title:	Project Work
Course Code: BDA 799	**Course Instructor:**
Academic Year: 2020 - 2021	**Semester:** Second Year, Semester 3, 4
No of Credits: 25	**Prerequisites:** SDLC, Communication Skills, technical skills.

Synopsis:	The project work aims to challenge analytical, creative ability and to allow students to synthesize, apply the expertise and insight learned in the core discipline. Students build self-confidence, demonstrate independence, and develop professionalism on successfully completion of the project.
Course Outcomes (COs):	On successful completion of this course, students will be able to
CO 1:	To be acquainted with working environment and processes that in place at the relevant Industries.
CO 2:	To familiarize the challenges as relevant professionals.
CO 3:	Review the literature and develop solutions for real time onboard projects.
CO 4:	Write technical report and deliver presentation.
CO 5:	Apply engineering and management principles to achieve project goal.

Mapping of COs to POs

COs	*PO 1*	*PO 2*	*PO 3*	*PO 4*	*PO 5*	*PO 6*	*PO 7*	*PO 8*	*PO 9*	*PO 10*	*PO 11*
CO 1						*	*	*	*	*	*
CO 2					*						
CO 3	*	*	*	*	*						
CO 4	*	*	*	*							
CO5:						*	*	*	*	*	*

Course content and outcomes:

Content	***Competencies***
Phase 1:	

Problem identification, synopsis submission, status submission, mid evaluation.	At the end of the topic student should be able to: 1. Identify the problem/specification (C1) 2. Discuss the project (C2) 3. Prepare the outline (C3) 4. Prepare a mid-term project presentation report (C3) 5. Prepare and present mid-term project presentation slides (C5) 6. Develop project implementation in hardware/software or both in chosen platform (C5)
Phase 2	
Status submission, final evaluation.	1. Prepare the progress report (C3) 2. Prepare the final project presentation report (C3) 3. Prepare and present final project presentation slides (C5) 4. Modify and Develop implementation in hardware/software or both in chosen platform (C5) 5. Justify the methods used and obtained results (C6)

Learning strategies, contact hours and student learning time

Learning strategy	*Contact hours*	*Student learning time (Hrs)*
Lecture	-	-
Seminar	-	-
Quiz	-	-
Small Group Discussion (SGD)	-	-

Self-directed learning (SDL)	-	-
Problem Based Learning (PBL)	-	-
Case Based Learning (CBL)	-	-
Clinic	-	-
Practical	-	-
Revision	-	-
Assessment	-	-
TOTAL	**-**	**-**

Assessment Methods:	
Formative:	**Summative:**
Project Problem Selection	Mid-Term Presentation
Synopsys review	Second status review
First status review	Demo & Final Presentation

Mapping of assessment with Cos					
Nature of assessment	CO 1	CO 2	CO 3	CO 4	CO 5
Mid Presentation	*	*			
Presentation	*	*	*	*	*

Feedback Process	• End-Semester Feedback
Reference Material	Particular to the chosen project

PROGRAM OUTCOMES (POS) AND COURSE OUTCMES (COS) MAPPING

Sl.No.	Course Code	Course Name	Credits	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
1	CSE 606	Data Structures	3	*	*		*		*					
2	EDA 601	High Level Digital Design	3	*	*	*								
3	EDA 602	Digital Systems & VLSI Design	3	*	*	*	*							
4	EDA 603	Verification	3	*	*	*	*							
5	EDA-608	System on Chip Design	3	*	*	*								
6	EDA-609	CAD for VLSI	3	*	*	*	*	*						
7	ESD-603	Digital Signal Processing	3	*	*	*	*	*						
8	CSE 606L	Data Structures Lab	1		*	*		*			*			
7	EDA 601L	High Level Digital Design Lab	1	*	*	*		*						
8	EDA 602L	Digital Systems & VLSI Design Lab	1	*	*	*		*						
9	EDA 603L	Verification Lab	1	*	*	*	*	*						
10	EDA-608L	System on Chip Design Lab	1	*	*			*	*	*				
11	EDA-609L	CAD for VLSI Lab	1	*	*	*	*	*						
12	ESD-603L	Digital Signal Processing Lab	1	*	*		*	*						
13	EDA 695	Mini Project - 1	4				*	*	*	*	*		*	*
14	EDA 697	Seminar - 1	1	*							*	*		*
15	EDA 604	Advanced VLSI Design	3	*	*	*								

16	EDA 605	Low Power VLSI Design	3	*	*	*	*	*						
17	EDA 606	Universal Verification Methodology	3	*	*	*								
18	EDA 607	Scripting for VLSI	3	*	*	*	*							
19	CSE-631	IT Project Management	3	*	*	*								
20	EDA-610	Physical Design	3	*	*	*								
21	EDA-611	Advanced Logic Synthesis	3	*	*	*								
22	EDA-613	Wireless Communications and Antenna Design	3	*	*	*	*							
23	EDA-614	Machine Learning for VLSI Design	3	*	*	*	*							
24	ENP-601	Entrepreneurship	3	*		*	*		*		*		*	
25	EDA 604L	Advanced VLSI Design Lab	1	*	*		*	*	*					
26	EDA 605L	Low Power VLSI Design Lab	1	*	*	*	*	*						
27	EDA 606L	Universal Verification Methodology Lab	1	*	*	*		*						
28	EDA 607L	Scripting for VLSI Lab	1	*		*		*						
29	CSE-631L	IT Project Management Lab	1			*	*	*				*		
30	EDA-610L	Physical Design Lab	1	*	*	*		*	*		*			
31	EDA-611L	Advanced Logic Synthesis Lab	1	*	*	*		*	*					
32	EDA-613L	Wireless Communications and Antenna Design Lab	1					*	*	*				

33	EDA-614L	Machine Learning for VLSI Design Lab	1					*	*	*				
34	ENP-601L	Entrepreneurship Lab	1	*					*	*	*		*	
35	EDA 696	Mini Project - 2	4				*	*	*	*	*		*	*
36	EDA 698	Seminar - 2	1	*							*	*		*
37	EDA 799	Project Work	25	*	*	*	*	*	*	*	*	*	*	*